

NASA CR-132465
ERIM 195800-25-F

**MIDAS, PROTOTYPE MULTIVARIATE INTERACTIVE
DIGITAL ANALYSIS SYSTEM – PHASE I**

Volume III: Wiring Diagrams

by

F. J. Kriegler, et al.
Infrared and Optics Division

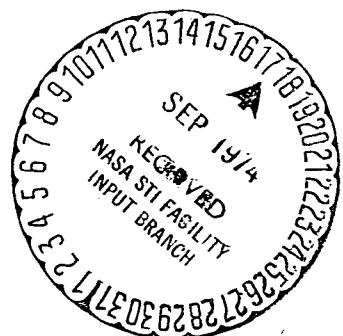


August 1974

prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Langley Research Center
Hampton, VA 23665
Contract No. NAS1-11979



TECHNICAL REPORT STANDARD TITLE PAGE

1. Report No. NASA CR-132465	2. Government Accession No.	3. Recipient's Catalog No.	
4. Title and Subtitle MIDAS, PROTOTYPE MULTIVARIATE INTERACTIVE DIGITAL ANALYSIS SYSTEM—PHASE I VOLUME III: WIRING DIAGRAMS		5. Report Date August 1974	
7. Author(s) <u>F. J. Kriegler et al.</u>		6. Performing Organization Code	
9. Performing Organization Name and Address Infrared and Optics Division Environmental Research Institute of Michigan P.O. Box 618 Ann Arbor, MI 48107		8. Performing Organization Report No. 195800-25-F	
12. Sponsoring Agency Name and Address National Aeronautics and Space Administration Washington, D.C. 20546		10. Work Unit No.	
		11. Contract or Grant No. NAS 1-11979	
		13. Type of Report and Period Covered Final Report, October 1972 through February 1974	
15. Supplementary Notes Volume III of III.		14. Sponsoring Agency Code	
16. Abstract The MIDAS System is a third-generation, fast, multispectral recognition system able to keep pace with the large quantity and high rates of data acquisition from present and projected sensors. MIDAS, for example, can process a complete ERTS frame in forty seconds and provide a color map of sixteen constituent categories in a few minutes. A principal objective of the MIDAS Program is to provide a system well interfaced with the human operator and thus to obtain large overall reductions in turn-around time and significant gains in throughput. This goal is elaborated in this report as an objective of the Phase II program.			
This report describes the hardware and software generated in Phase I of the overall program. The system contains a mini-computer to control the various high-speed processing elements in the data path and a classifier which implements an all-digital prototype multivariate-Gaussian maximum likelihood decision algorithm operating at 2×10^5 pixels/sec. Sufficient hardware has been developed to perform signature extraction from computer-compatible tapes, compute classifier coefficients, control the classifier operation, and diagnose operation.			
Volume I describes the MIDAS System in detail; Volume II contains the diagnostic programs used to test MIDAS' operation; Volume III displays the MIDAS construction and wiring diagrams.			
17. Key Words Wirewrap A/D-D/A conversion Multispectral recognition system Multivariate-Gaussian maximum likelihood decision algorithm	18. Distribution Statement Initial distribution listed at the end of this report Unclassified-Unlimited		
19. Security Classif. (of this report) UNCLASSIFIED	20. Security Classif. (of this page) UNCLASSIFIED	21. No. of Pages 85	22. Price

PREFACE

A comprehensive multispectral program devoted to the advancement of state-of-the-art techniques for remote sensing of the environment has been a continuing program at the Environmental Research Institute of Michigan (ERIM), formerly the Willow Run Laboratories of The University of Michigan. The basic objective of this multidisciplinary program is to develop remote sensing as a practical tool to provide the user with processed information quickly and economically.

The importance of providing timely information obtained by remote sensing to such people as the farmer, the city planner, the conservationist, and others concerned with problems such as crop yield and disease, urban land studies and development, water pollution, and forest management must be carefully considered in the overall program. The scope of our program includes: (1) extending the understanding of basic processes; (2) discovering new applications; (3) developing advanced remote-sensing systems; (4) improving fast automatic data processing systems to extract information in a useful form; and also (5) assisting in data collection, processing, analysis and ground truth verification. The MIDAS program applies directly to No. (4) with its improved data processing capability.

This document is the final report for Phase I of the MIDAS program under NASA Contract NAS1-11979 and covers the period from October 1972 through February 1974. The contract effort was monitored by Mr. William Howle of NASA-Langley. The overall program is guided by Mr. R. R. Legault, Vice President of ERIM, and Director of the Infrared and Optics Division. Work on this contract was directed by J. D. Erickson, Head of the Multispectral Analysis Section, and by F. J. Kriegler, Principal Investigator. The ERIM number for this report is 195800-25-F.

ERIM personnel who contributed to this project and who co-authored this report are Dempster Christenson, Michael Gordon, Roland Kistler, Seymour Lampert, Robert Marshall, and Rowland McLaughlin. In addition to providing the text, their individual contributions were as follows: Dempster Christenson and Michael Gordon provided system programming and diagnostic software; Roland Kistler and Seymour Lampert provided the detailed design and performed system checkout; Robert Marshall aided in overall system configuration; Rowland McLaughlin organized this report. The authors wish to acknowledge the direction provided by Mr. R. R. Legault and Dr. J. D. Erickson. Outstanding contributions were made by the following persons: John Baumler, Clyde Connell, William Juodawlkis, Robert Pierson, Cary Wilson, and Nancy Wilson for their efforts in system construction.

Page Intentionally Left Blank

CONTENTS

1. INTRODUCTION	1
2. GENERAL SYSTEM CONFIGURATION	2
3. CLASSIFIER SECTION	6
4. CONTROL AND HYBRID SECTION	35
5. BACKPLANE INTRA-BAY WIRING	63
6. SYSTEM CABLING	66
6.1 Cabling Between Hybrid and Control Bays	66
6.2 Cabling Between Classifier and Computer	66
DISTRIBUTION LIST	85

FIGURES

1. Block Diagram of the MIDAS System	3
2. Location of Major MIDAS Components	4
3. Block Diagram of the Quadratic Pipe	5
4. Block Diagram of the Mean Card	7
5. Block Diagram of the Variance Card	8
6. Block Diagram of the Matrix Multiplier Card	9
7. Block Diagram of the Square Card	10
8. Block Diagram of the Square-Accumulator Card	11
9. Block Diagram of the Diagnostic/Output Card	12
10. Block Diagram of the Clock Card	13
11. Block Diagram of the k^2 Card	14
12. Block Diagram of the Recognition Card	15
13. Mean (MN)	16
14. Variance (VAR)	18
15. 8×8 Matrix Multiplier (MTX)	20
16. 9×9 Square Card (SQ)	22
17. Square-Accumulator (SA)	24
18. Diagnostic/Output	26
19. Clock	29
20. k^2	31
21. Recognition	33
22. Control Section	36
23. Hybrid Bay Cards (H <u>(1-16)</u>)	37
24. Digital Input Synchronizer (C <u>(11,12)</u>)	38
25. Digital Output Synchronizer (C <u>(13,14)</u>)	39
26. Digital Data Selector (H <u>(19)</u>)	40
27. Hybrid Cards (H <u>(1-16)</u>)	41
28. Input Bus and Port Decoder (H <u>(17)</u>)	42
29. Output Bus and Port Decoder (H <u>(18)</u>)	43
30. Digital Data Selector (H <u>(19)</u>)	44
31. Analog Tape Recorder Control (C <u>(1)</u>)	45
32. Analog Line-Count Decoder (C <u>(2)</u>)	46
33. Line-Count Start/Stop (C <u>(3)</u>)	47
34. Digital Line-Count Decoder (C <u>(4)</u>)	48

35. Video and Calibration Generator (C <u>6,7</u>)	49
36. A/D-D/A Clock Generator (C <u>8</u>)	50
37. D/A Line-Count Clock (C <u>9</u>)	51
38. D/A Duty Cycle Generator (C <u>10</u>)	52
39. Digital Input Programmer I (C <u>11</u>)	53
40. Digital Input Programmer II (C <u>12</u>)	54
41. Digital Output Programmer I (C <u>13</u>)	55
42. Digital Output Programmer II (C <u>14</u>)	56
43. System Conditioner I (C <u>15</u>)	57
44. System Conditioner II (C <u>16</u>)	58
45. A/D Line-Control, Digital Transfer Control, and DR-11C Transfer Logic (C <u>17</u>)	59
46. A/D Word Transfer (C <u>18</u>)	60
47. Delay-Gate Generator (C <u>19</u>)	61
48. Playback Sync and Line-Count Clock Generator (C <u>20</u>)	62
49. Backplane Intra-Bay Wiring	64
50. System-Cabling Diagram	67
51. Physical Layout of Plug Card <u>(1-H)</u>	68
52. Output Connector Wiring of Plug Card <u>(1-H)</u>	69
53. Wiring of Plug Card <u>(2-H)</u>	70
54. Physical Layout of Plug Cards <u>(2-H)</u> and <u>(2-C)</u>	71
55. Plug Card <u>(1-C)</u>	72
56. DEC Block Layout	75
57. Wiring of Card <u>(2-C)</u>	76
58. Control Panel Wiring and Termination to Plug Card <u>(3-C)</u>	77
59. Physical Layout of Plug Card <u>(4-C)</u>	78
60. Wiring of Card <u>(4-C)</u>	79
61. Cable Terminations for Data Transfer from Computer to Classifier	81
62. Cable Terminations for Data Transfer to Computer from Classifier.	82
63. Inter-Bay Wiring	83



FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN

MIDAS, PROTOTYPE MULTIVARIATE INTERACTIVE DIGITAL ANALYSIS
SYSTEM—PHASE I

Volume III: Wiring Diagrams

1

INTRODUCTION

This volume contains block diagrams and schematics detailing the construction of the MIDAS Classifier. Their organization forms a tree structure in which the more general block diagrams reference the more detailed block diagrams which lead to the schematics. This provides a self-explanatory set of diagrams enabling the reader to acquaint himself with system design and circuitry to any desired level of detail.

2

GENERAL SYSTEM CONFIGURATION

The Phase-I MIDAS System is most easily visualized if organized into subsystems as shown in the block diagram of Fig. 1. The system is under complete control of the Digital Equipment Corporation (DEC) PDP-11/45 computer system. All control inputs by an operator are made by way of the computer keyboard. All commands are translated by computer software into code words and sent out over interface devices to set up the hardware registers in the special-purpose processor. These codes are decoded in three of the blocks shown in Fig. 1. These three places are: (1) in the control section, (2) in the clock section, and (3) in the Diagnostic/Output section. These codes will be described in detail in subsequent sections.

The MIDAS System is housed in one 6-foot rack. The physical location of the major components is shown in Fig. 2. Each of the 4 quadratic pipes is housing in a wire-wrap card file containing 13 wire-wrap circuit boards. The quadratic calculation is accomplished by a set of 12 boards in each bay while the other board in each bay is different as shown in Fig. 2.

High-speed mass data is transferred to and from the computer by means of (1) the A/D-D/A (hybrid) section, (2) the clock section, and (3) Diagnostic/Output section. High-speed multichannel data is transferred through the hybrid section and the quadratic computation pipes. The figure numbers shown in each of the blocks of Fig. 3 refer to more detailed figures describing that block.

The control bay and the hybrid bay have room for 22 circuit boards. There are 20 boards in the control bay numbered C-1 through C-20. There are 19 boards in the hybrid file numbered H-1 through H-19.

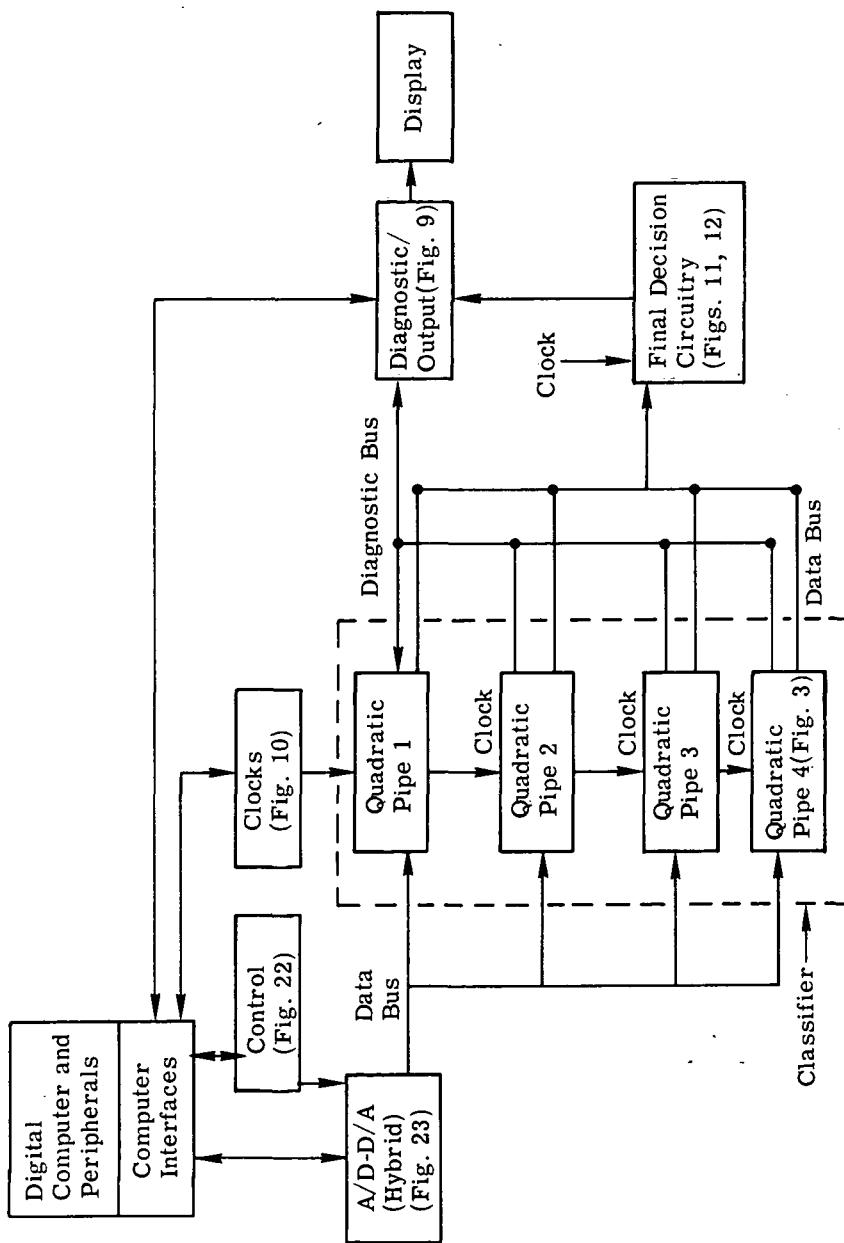


FIGURE 1. BLOCK DIAGRAM OF THE MIDAS SYSTEM

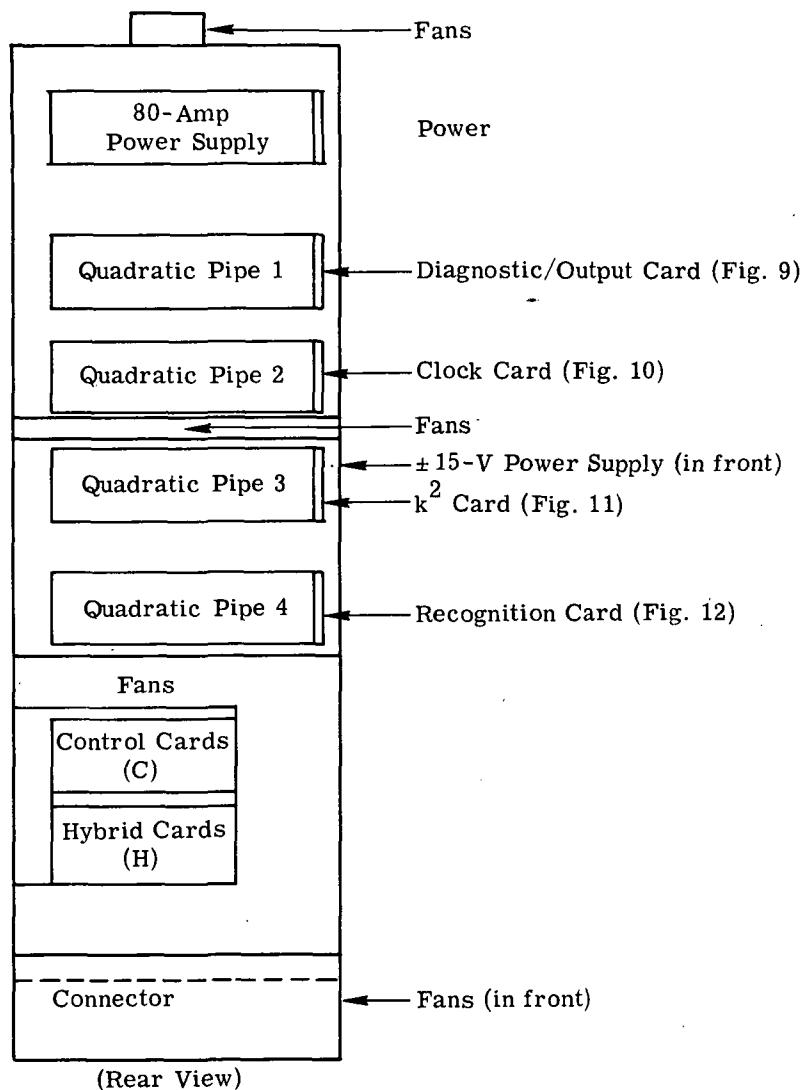


FIGURE 2. LOCATION OF MAJOR MIDAS COMPONENTS

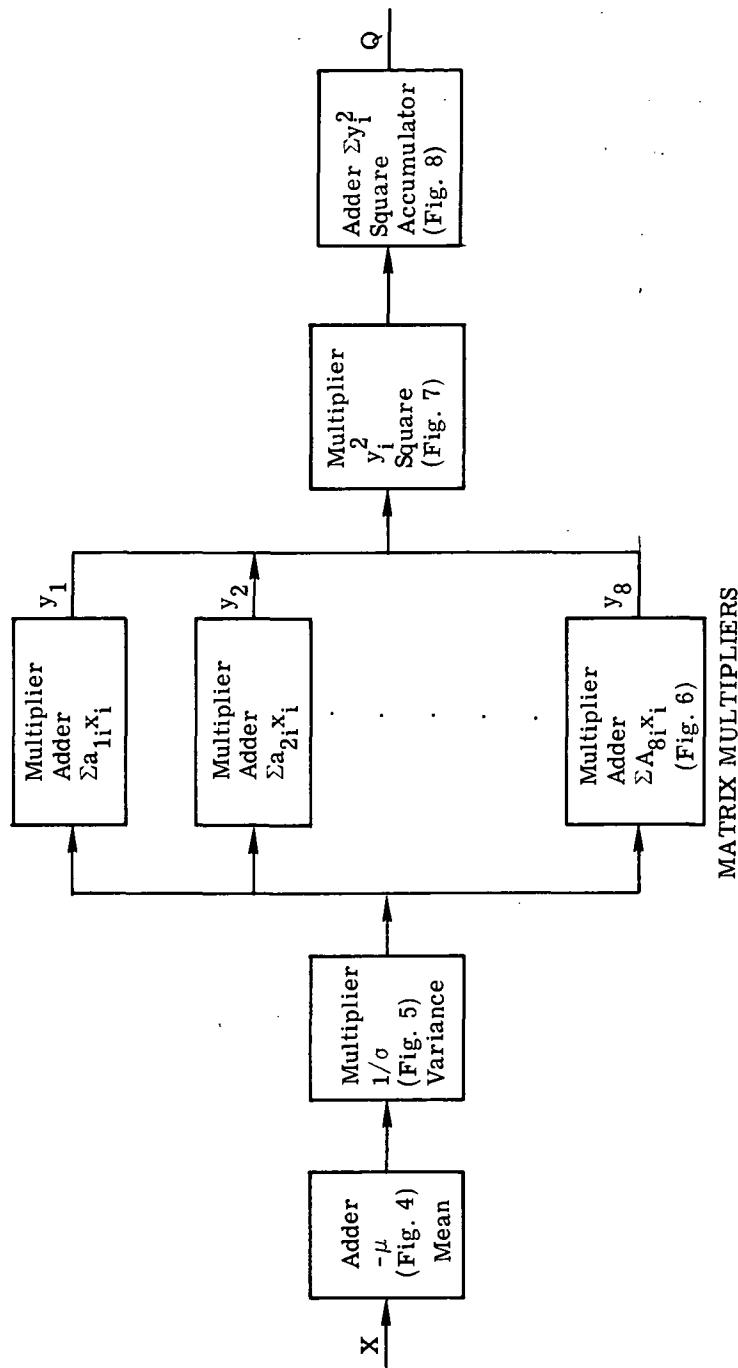


FIGURE 3. BLOCK DIAGRAM OF THE QUADRATIC PIPE

3
CLASSIFIER SECTION

A detailed description of the Classifier is given in Sections 4 and 6 of Volume I.

A block diagram of the quadratic pipe computation is shown in Fig. 3.

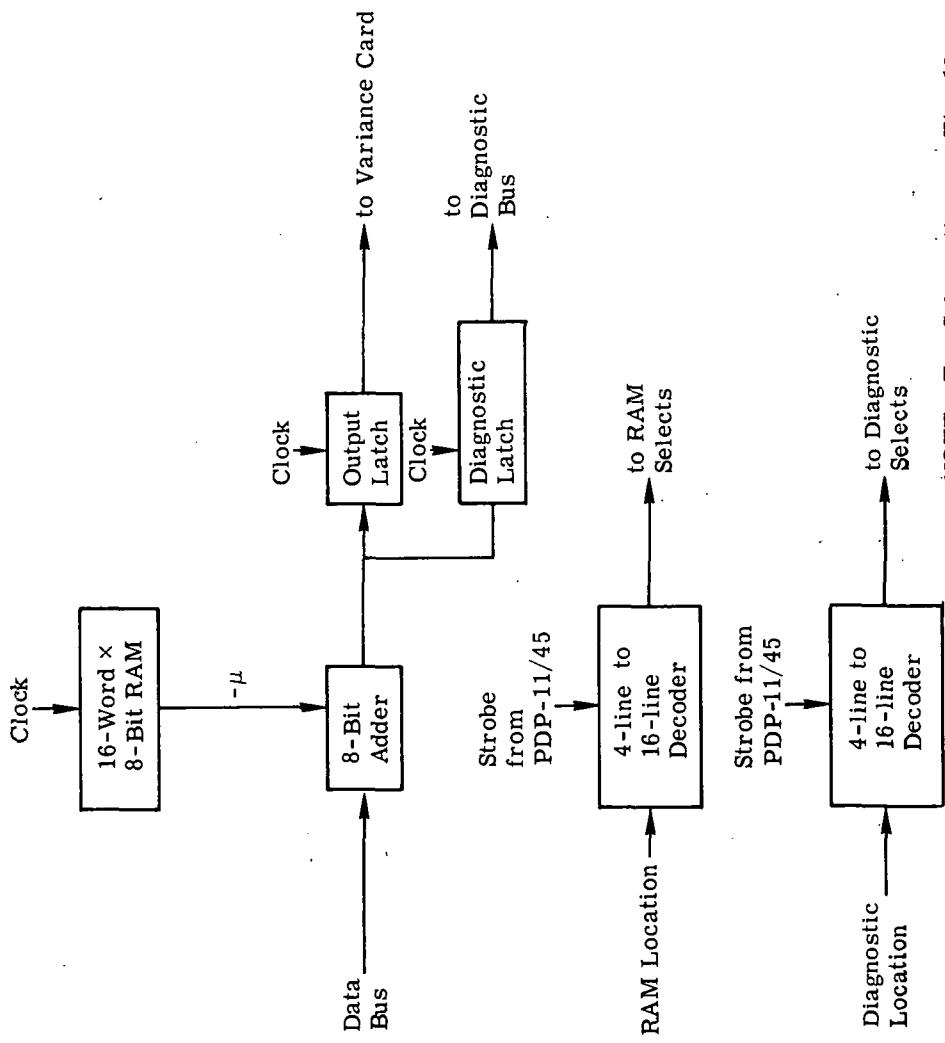
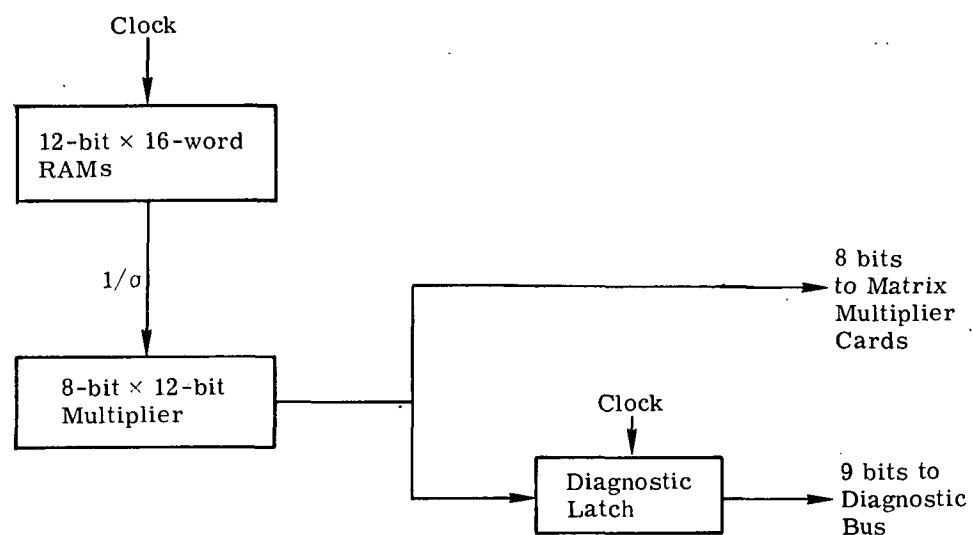


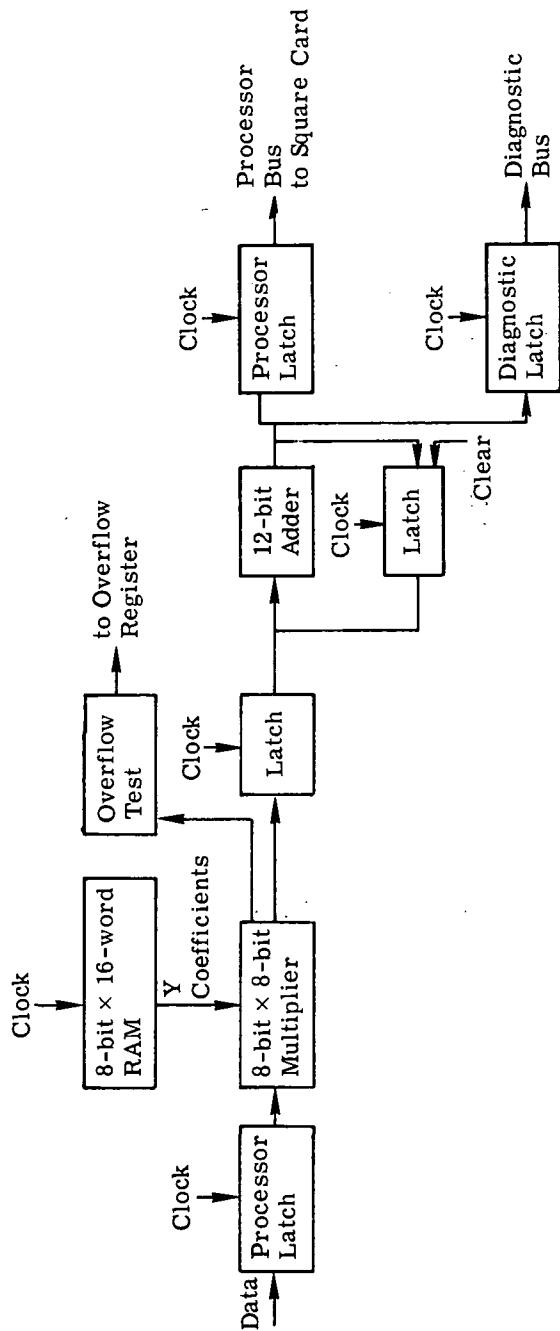
FIGURE 4. BLOCK DIAGRAM OF THE MEAN CARD

NOTE: For Schematic, see Fig. 13.



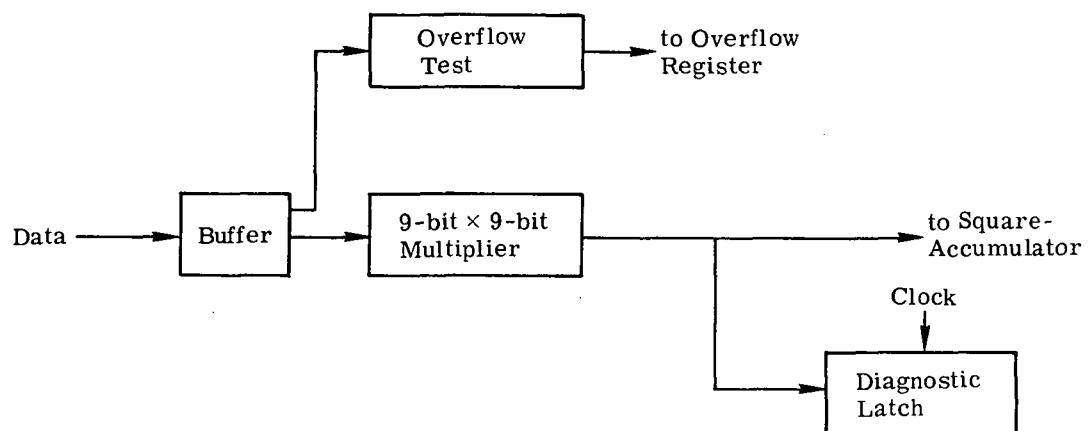
NOTE: For Schematic, see Fig. 14.

FIGURE 5. BLOCK DIAGRAM OF THE VARIANCE CARD



NOTE: For Schematic, see Fig. 15.

FIGURE 6. BLOCK DIAGRAM OF THE MATRIX MULTIPLIER CARD



NOTE: For Schematic, see Fig. 16.

FIGURE 7. BLOCK DIAGRAM OF THE SQUARE CARD

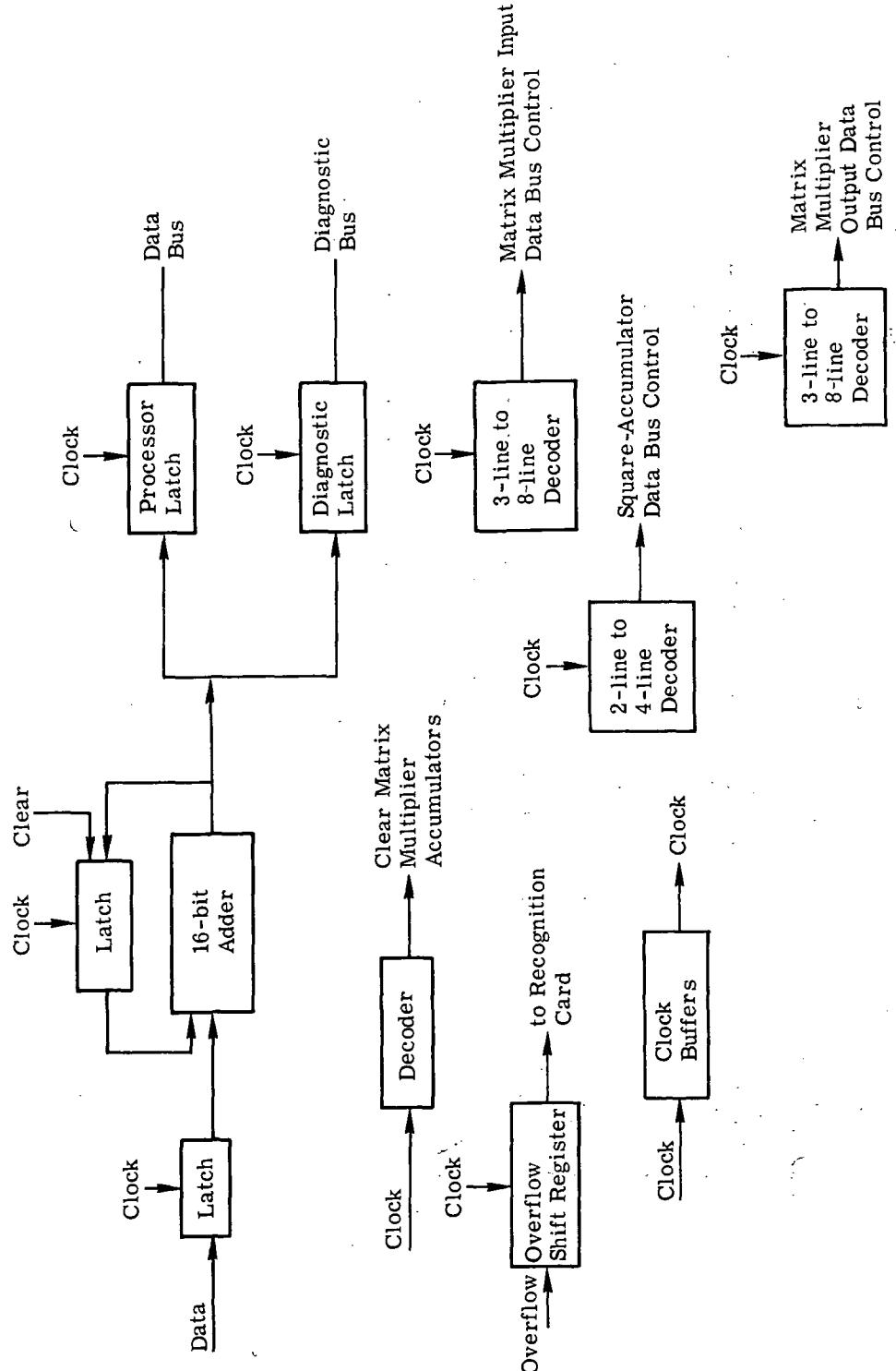


FIGURE 8. BLOCK DIAGRAM OF THE SQUARE-ACCUMULATOR CARD

NOTE: For Schematic, see Figure 17.

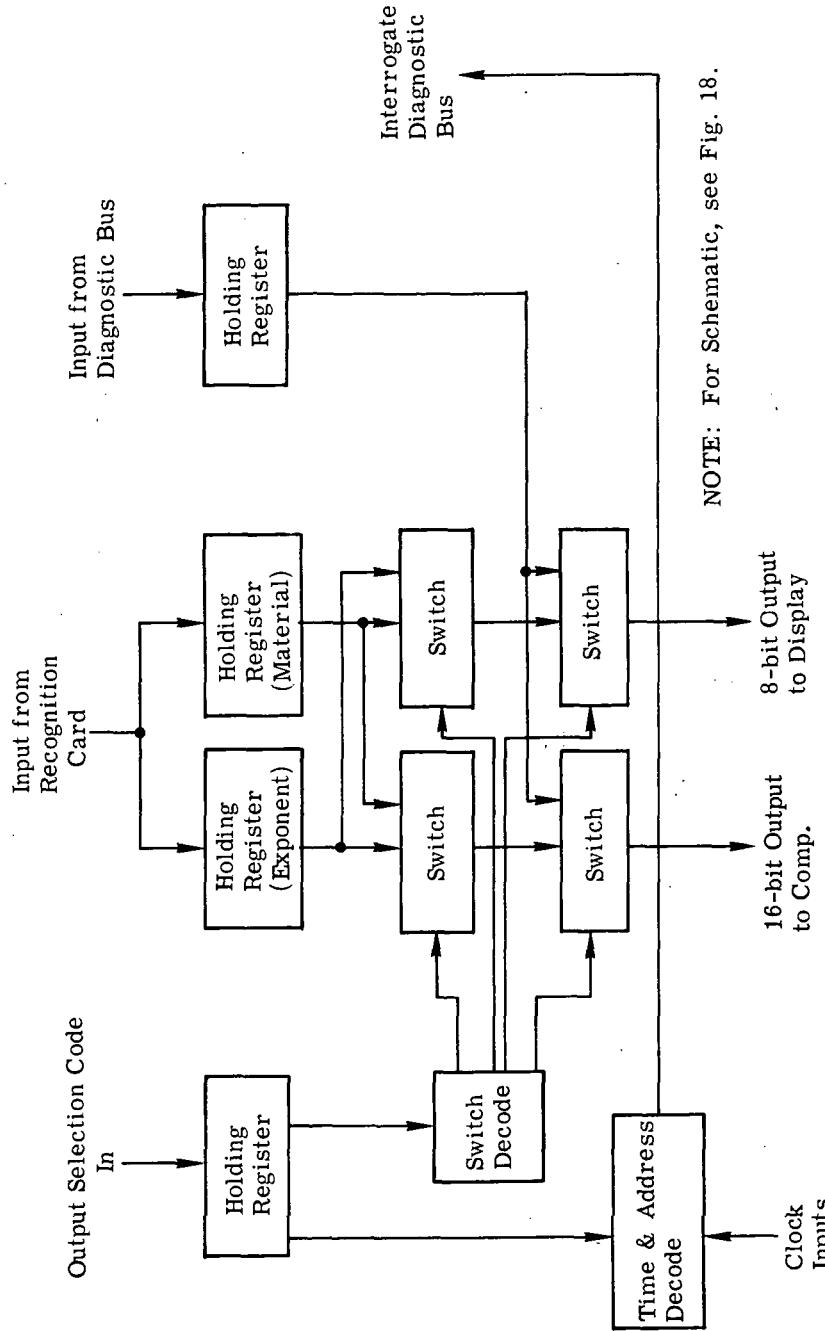
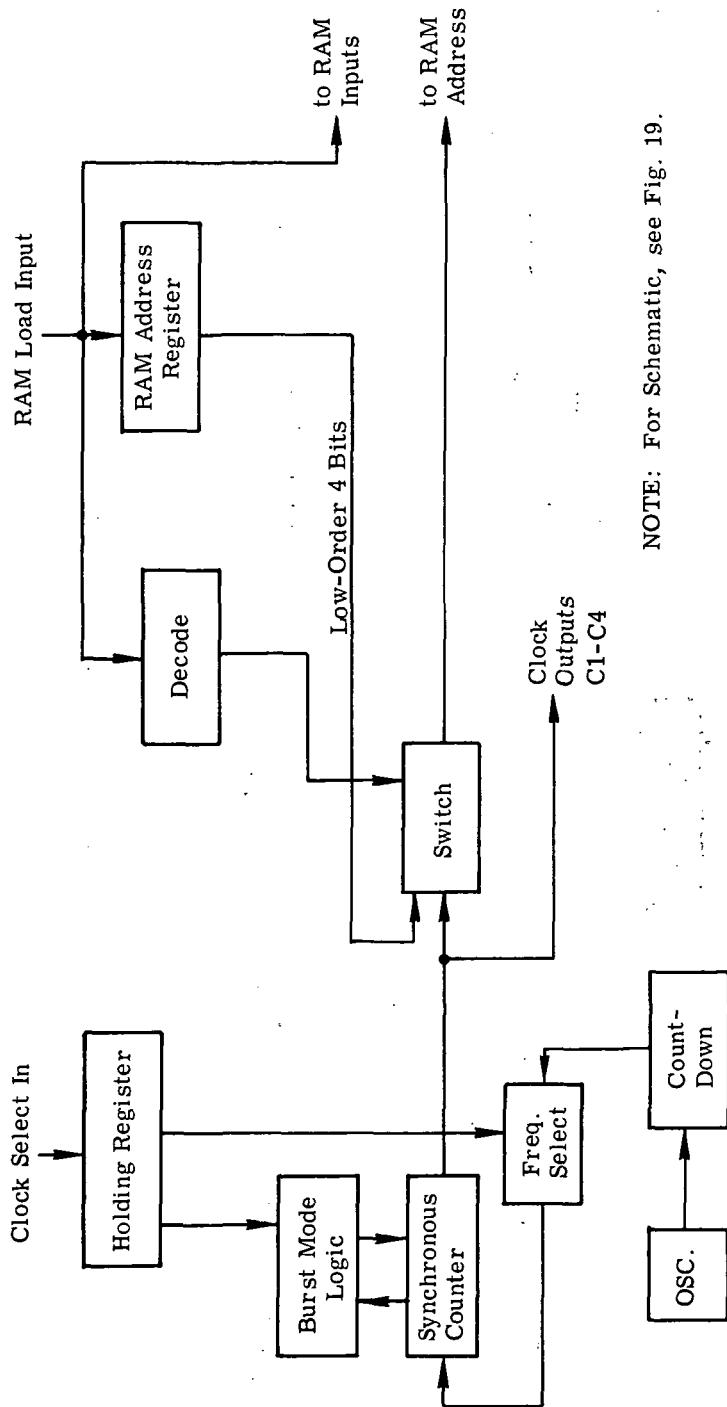
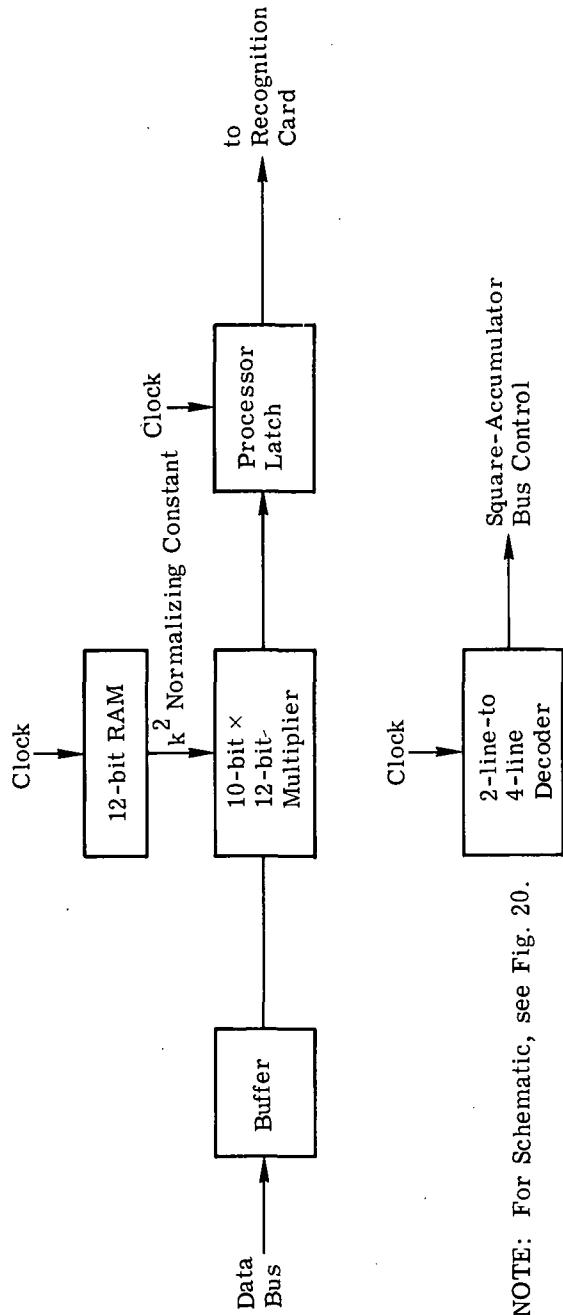


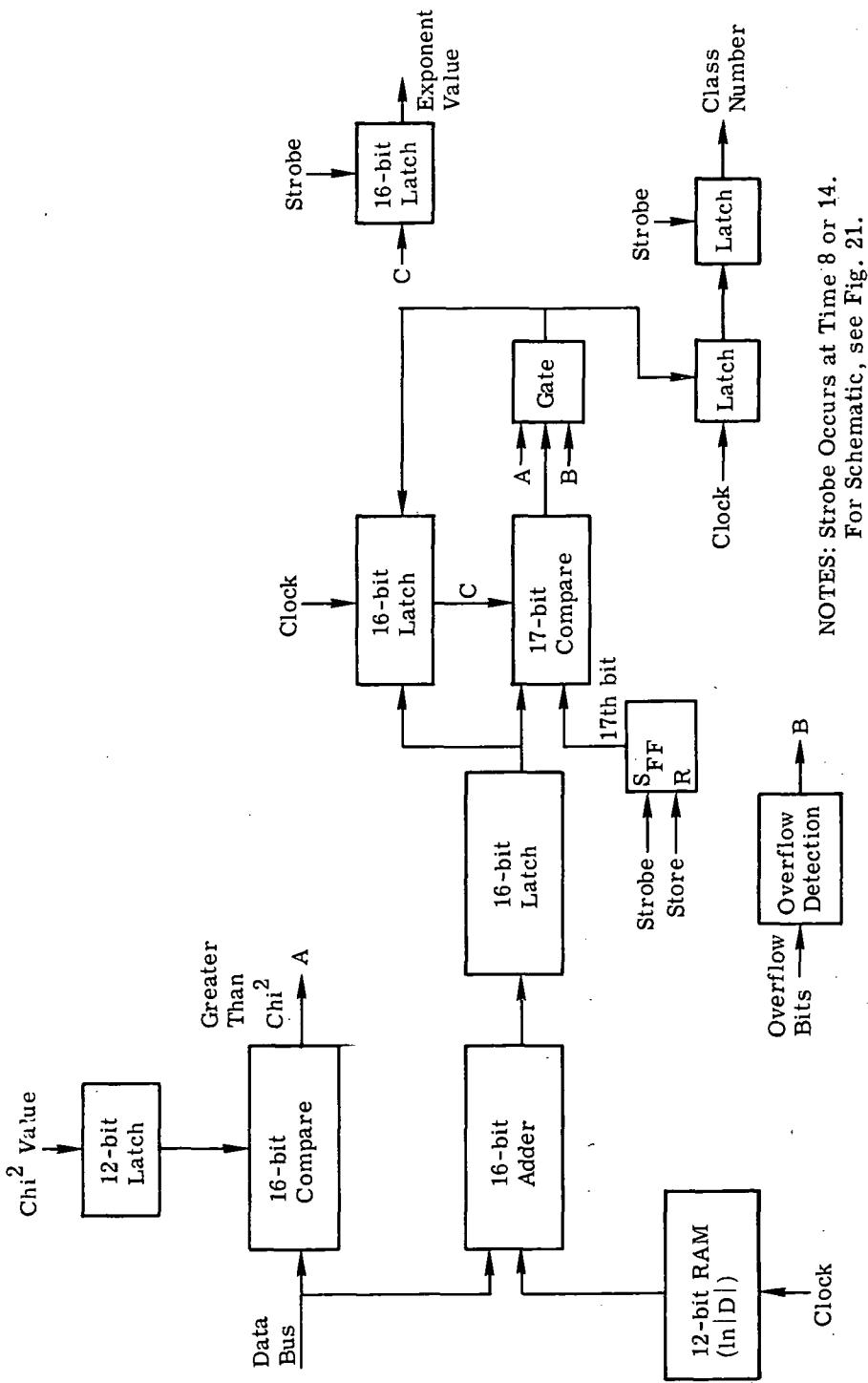
FIGURE 9. BLOCK DIAGRAM OF THE DIAGNOSTIC/OUTPUT CARD



NOTE: For Schematic, see Fig. 19.

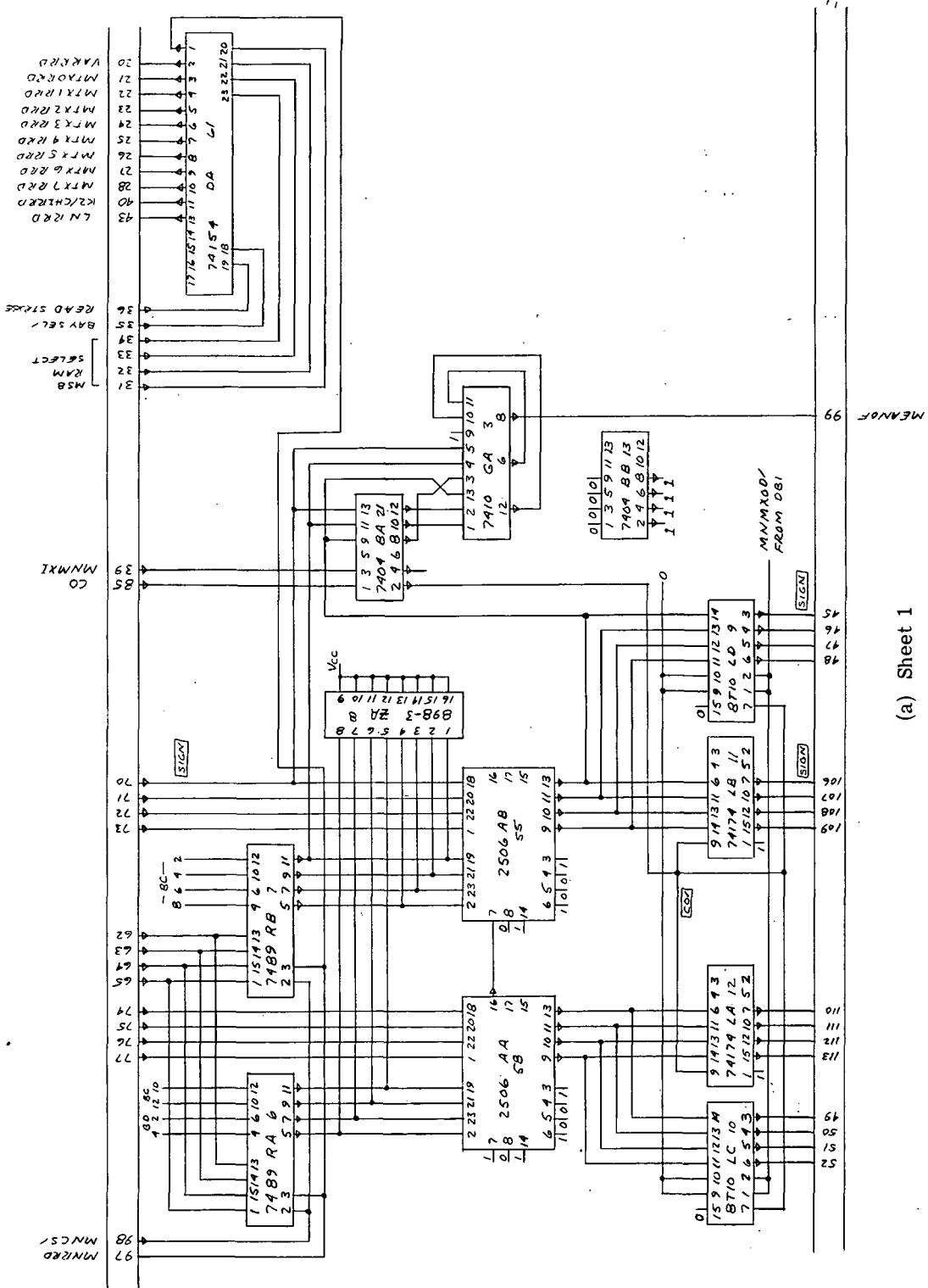
FIGURE 10. BLOCK DIAGRAM OF THE CLOCK CARD


 FIGURE 11. BLOCK DIAGRAM OF THE k^2 CARD



NOTES: Strobe Occurs at Time 8 or 14.
For Schematic, see Fig. 21.

FIGURE 12. BLOCK DIAGRAM OF THE RECOGNITION CARD

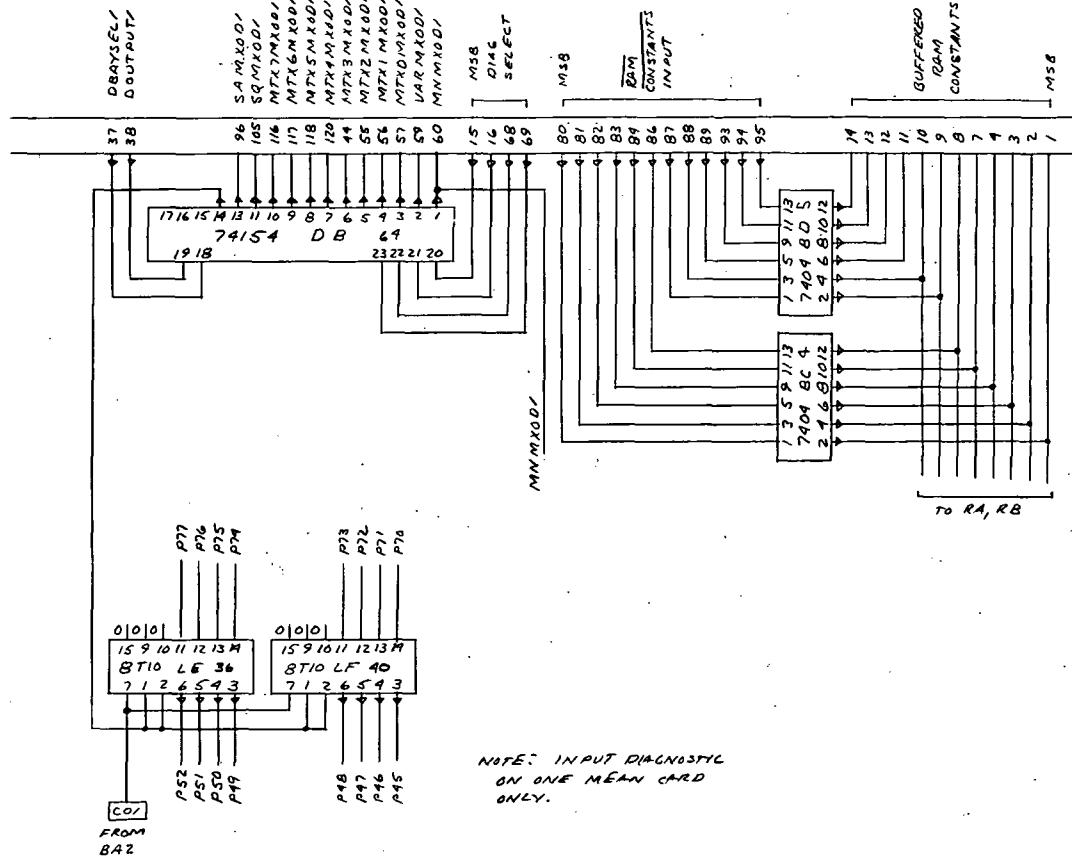


(a) Sheet 1

FIGURE 13. MEAN (MN) (Continued)



FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN

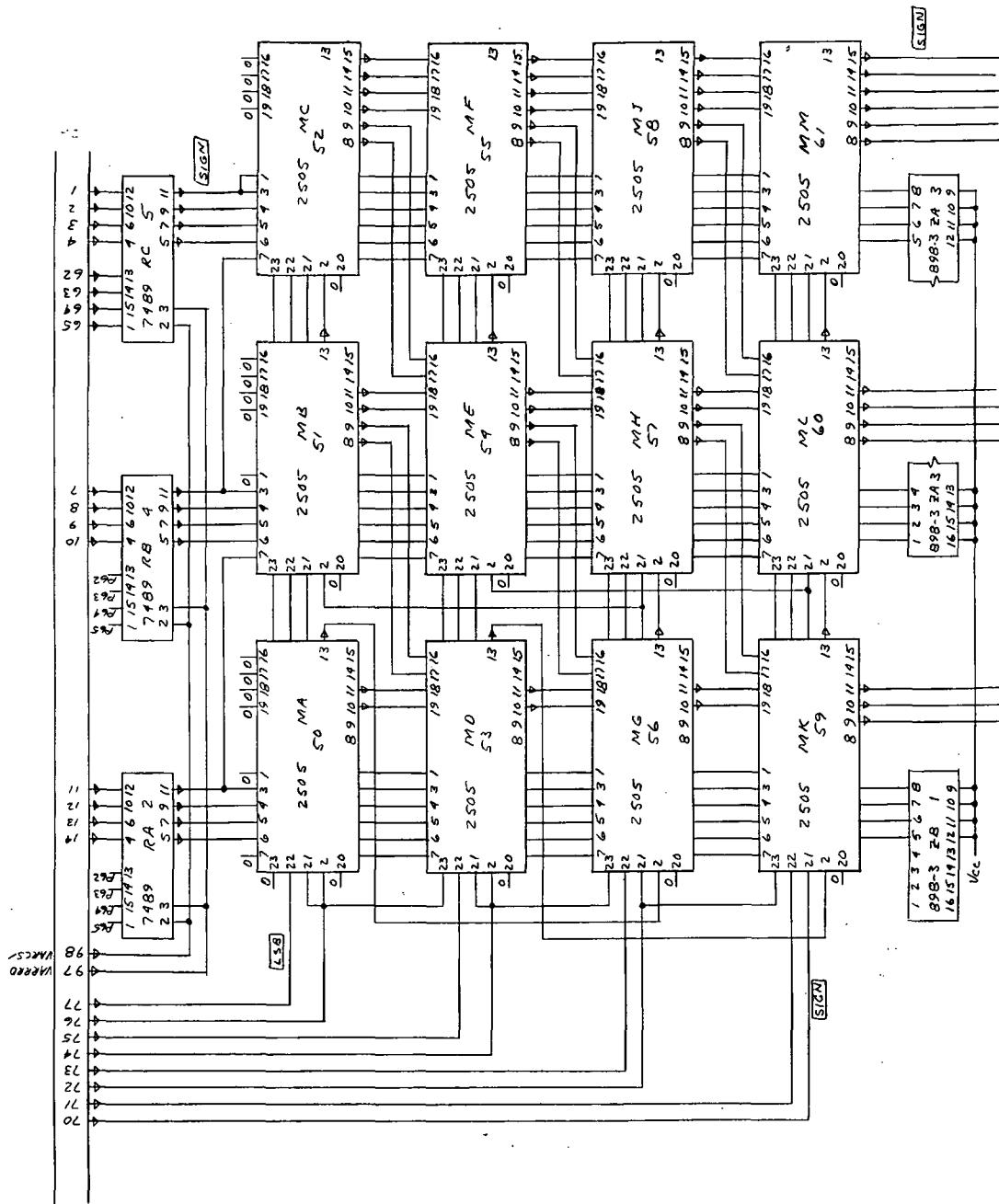


(b) Sheet 2

FIGURE 13. MEAN (MN) (Concluded)

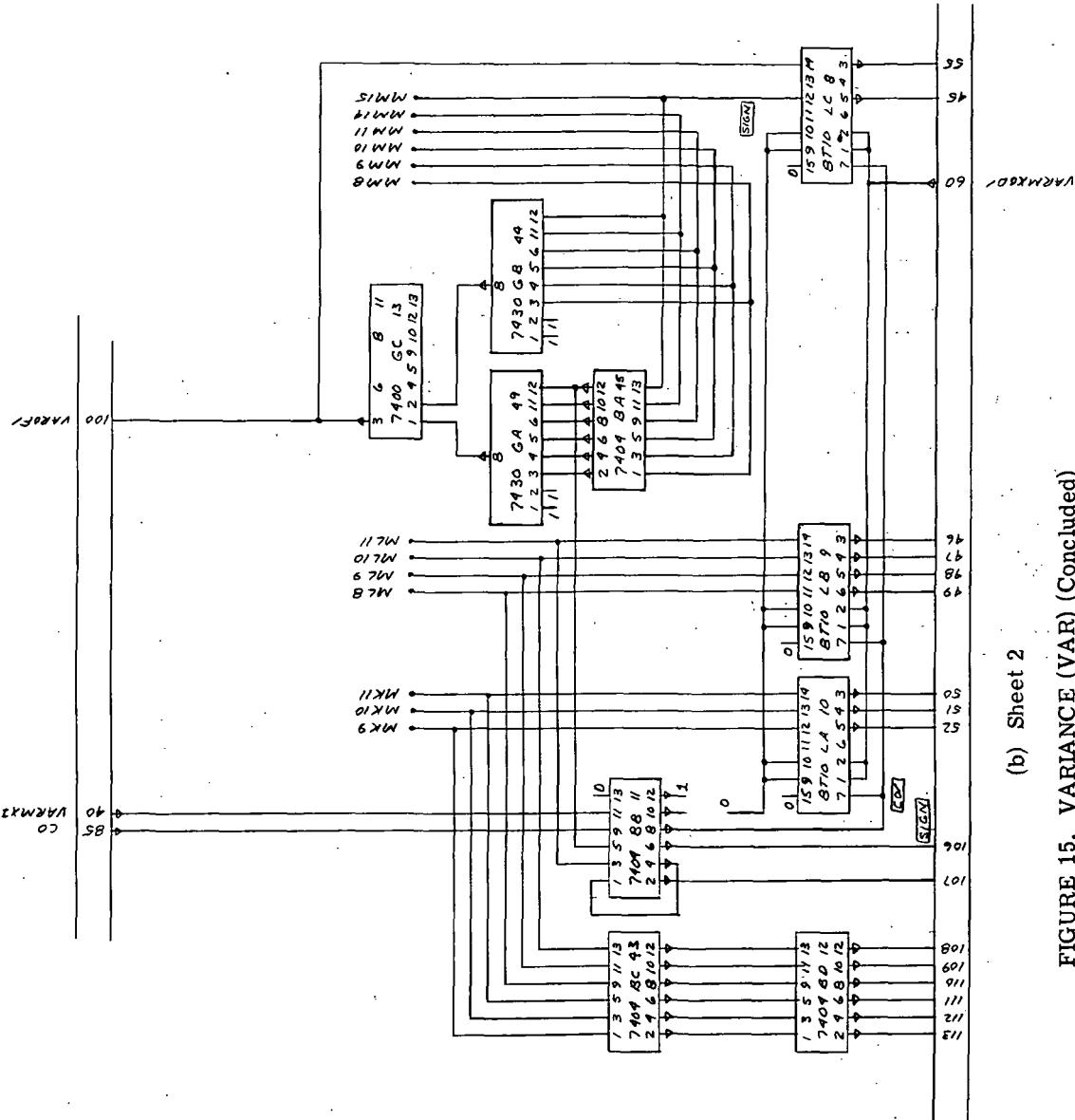


FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN



(a) Sheet 1

FIGURE 15. VARIANCE (VAR) (Continued)



(b) Sheet 2

FIGURE 15. VARIANCE (VAR) (Concluded)



FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN

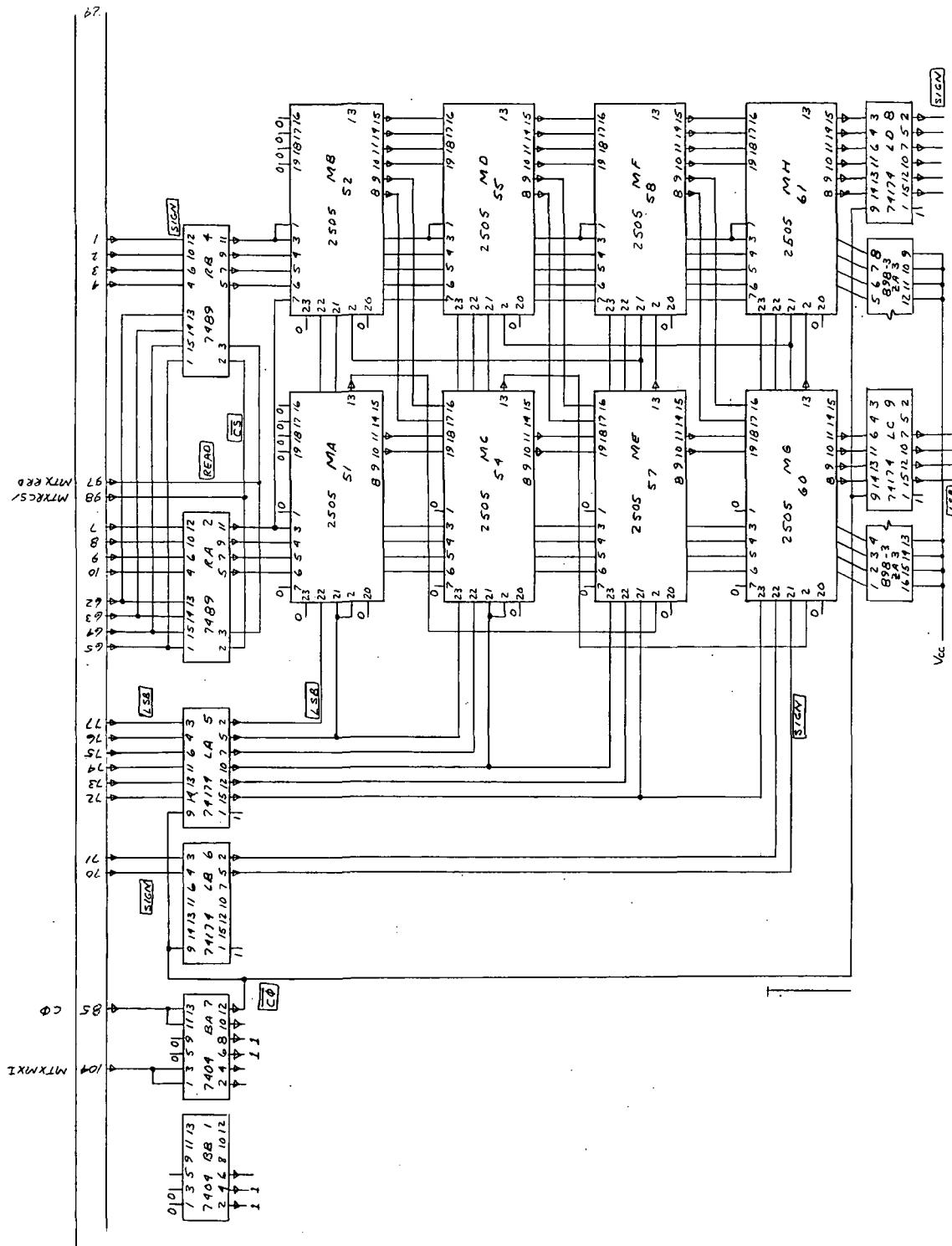
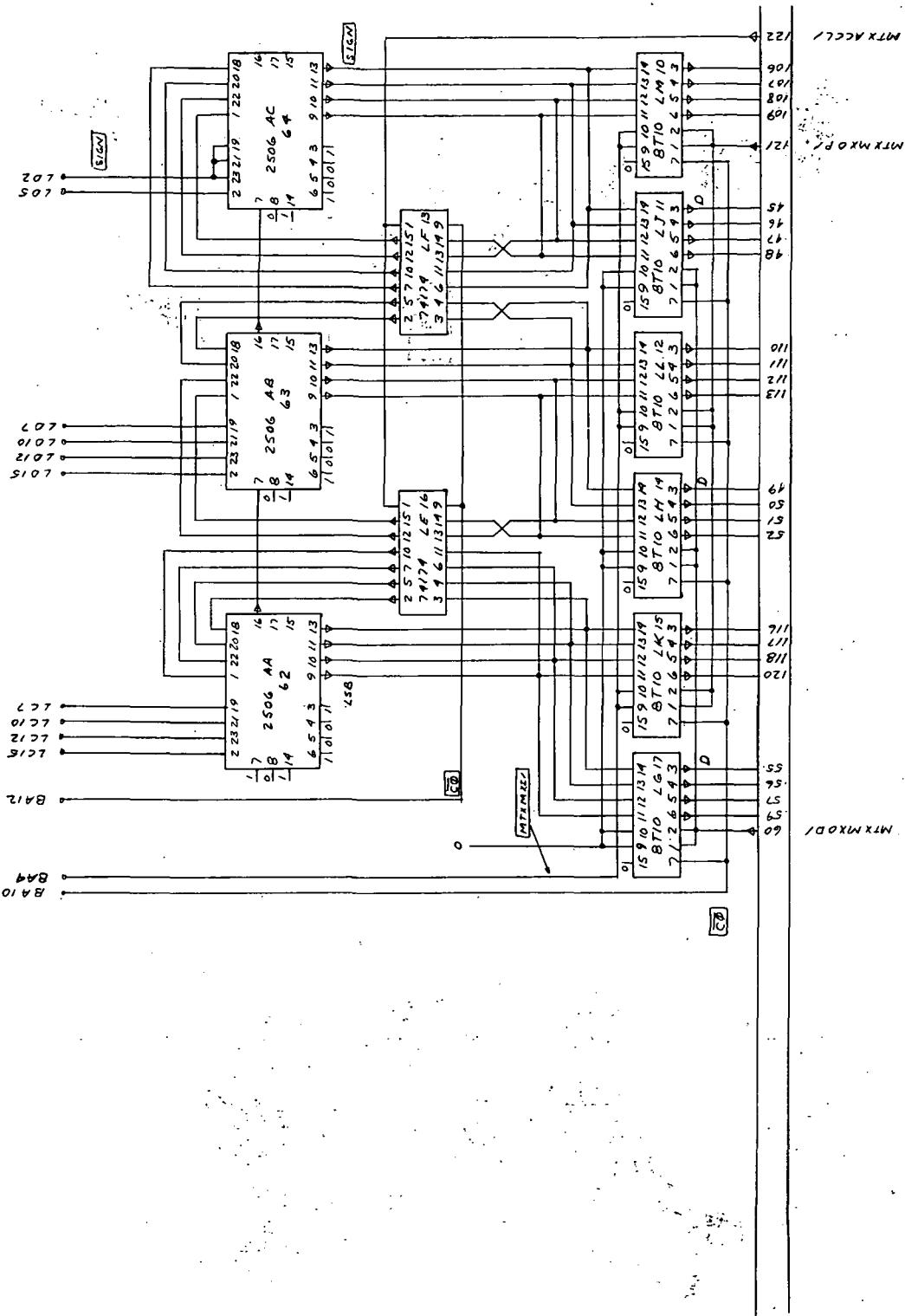


FIGURE 15. 8×8 MATRIX MULTIPLIER (MTX) (Continued)



(b) Sheet 2

FIGURE 15. 8 × 8 MATRIX MULTIPLIER (MTX) (Concluded)

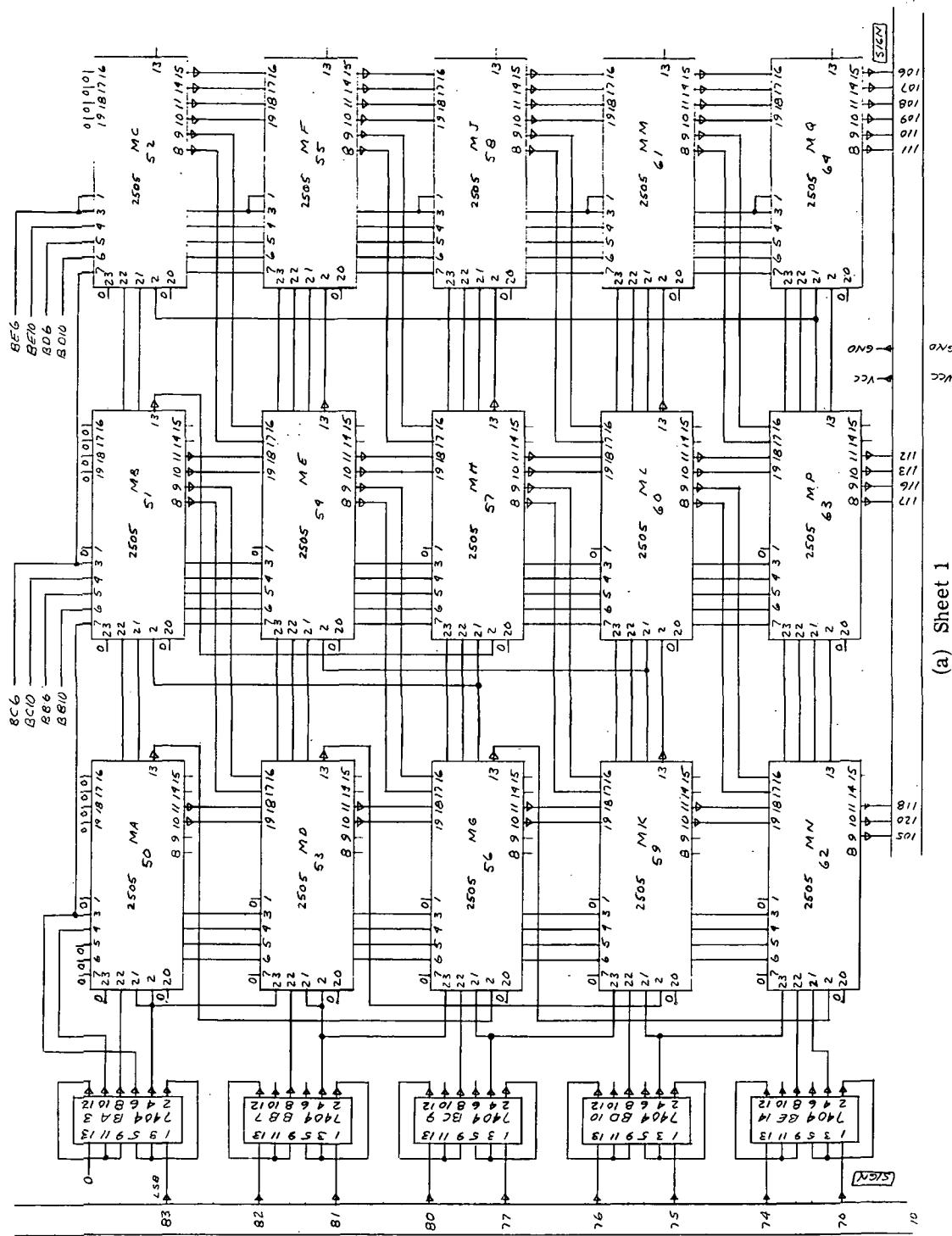


FIGURE 16. 9 × 9 SQUARE CARD (SQ) (Continued)

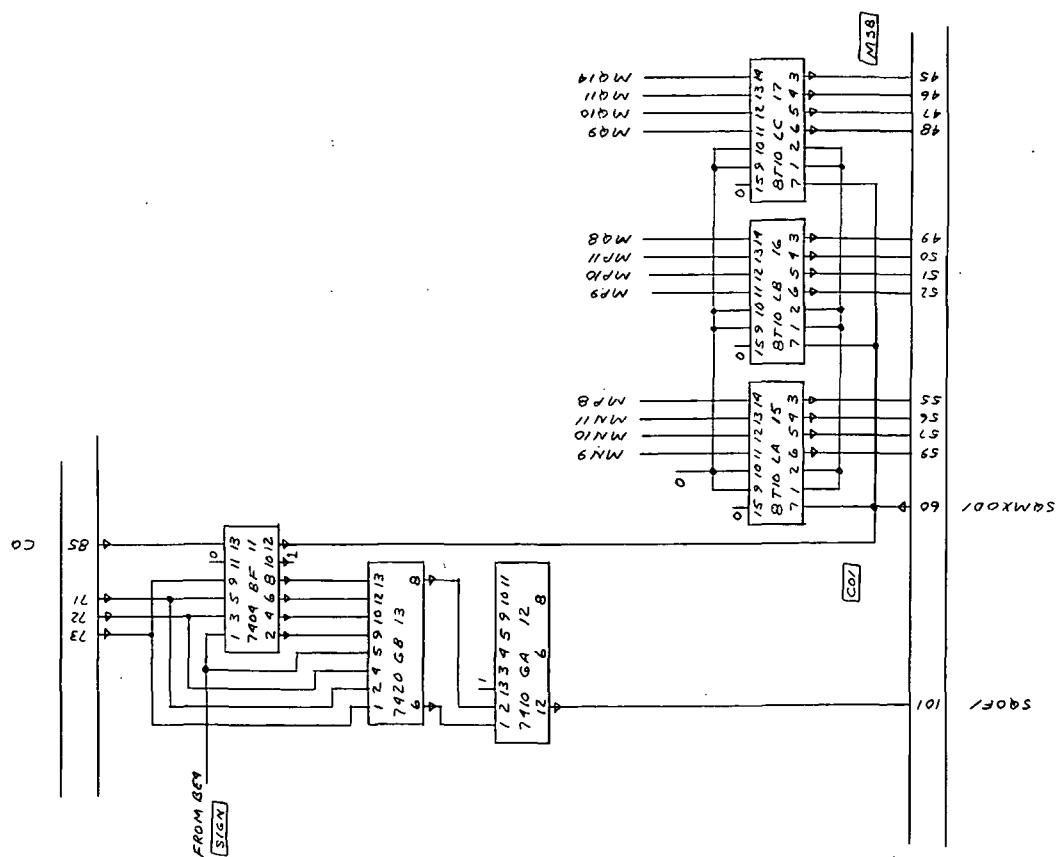
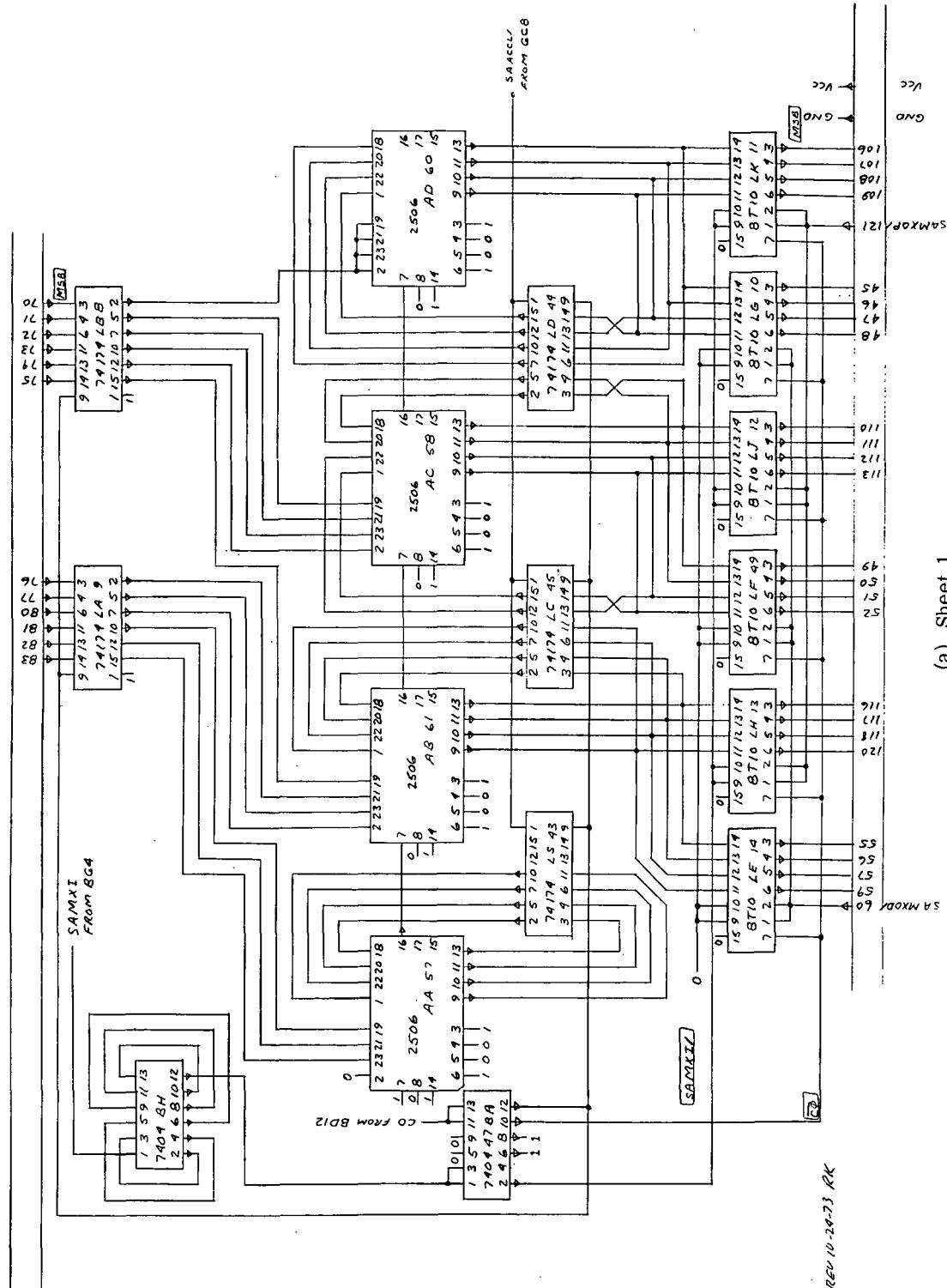


FIGURE 16. 9 x 9 SQUARE CARD (SQ) (Concluded)
 (b) Sheet 2

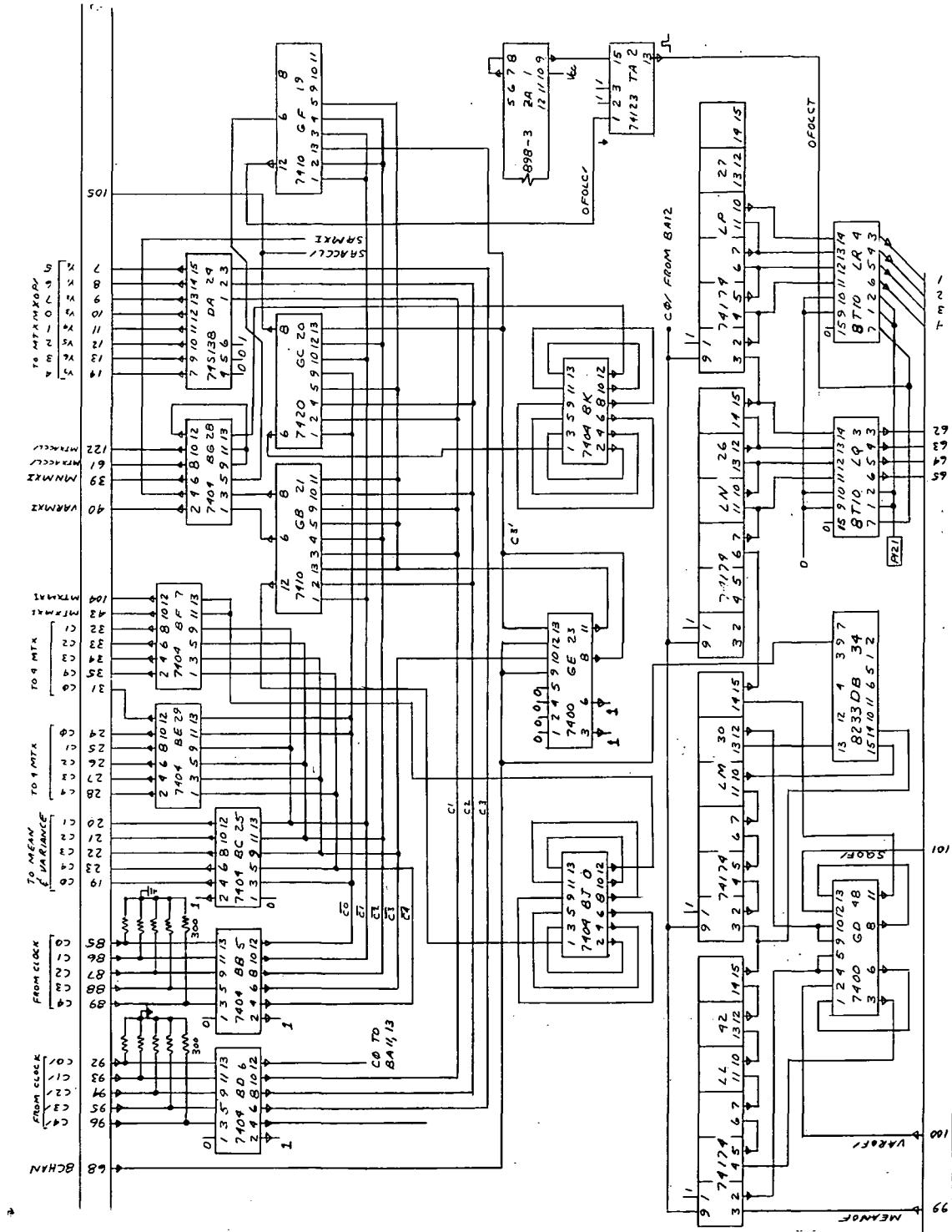


FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN



(a) Sheet 1

FIGURE 17. SQUARE-ACCUMULATOR (SA) (Continued)



(b) Sheet 2

FIGURE 17. SQUARE-ACCUMULATOR (SA) (Concluded)



FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN

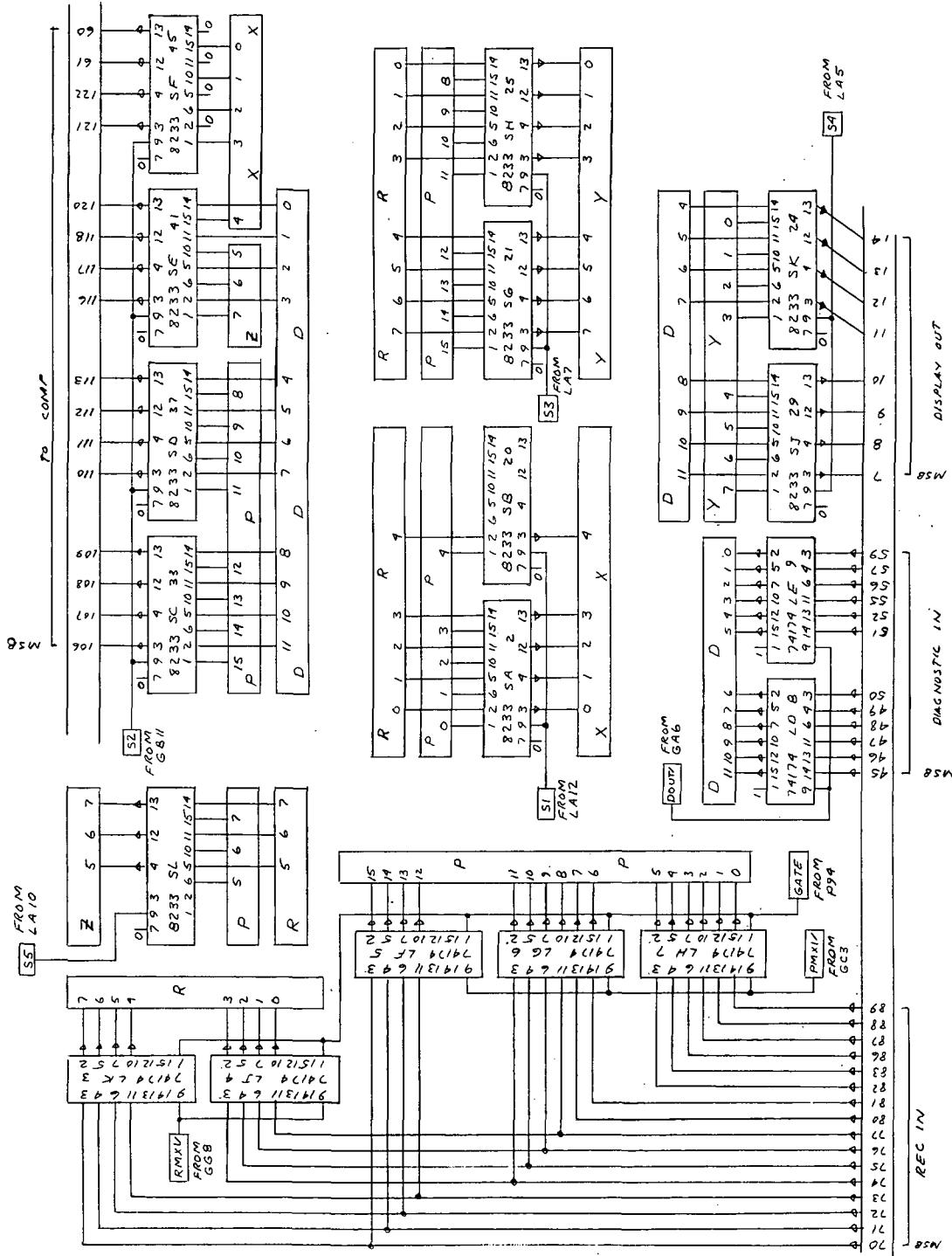


FIGURE 18. DIAGNOSTIC/OUTPUT (Continued)



FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN

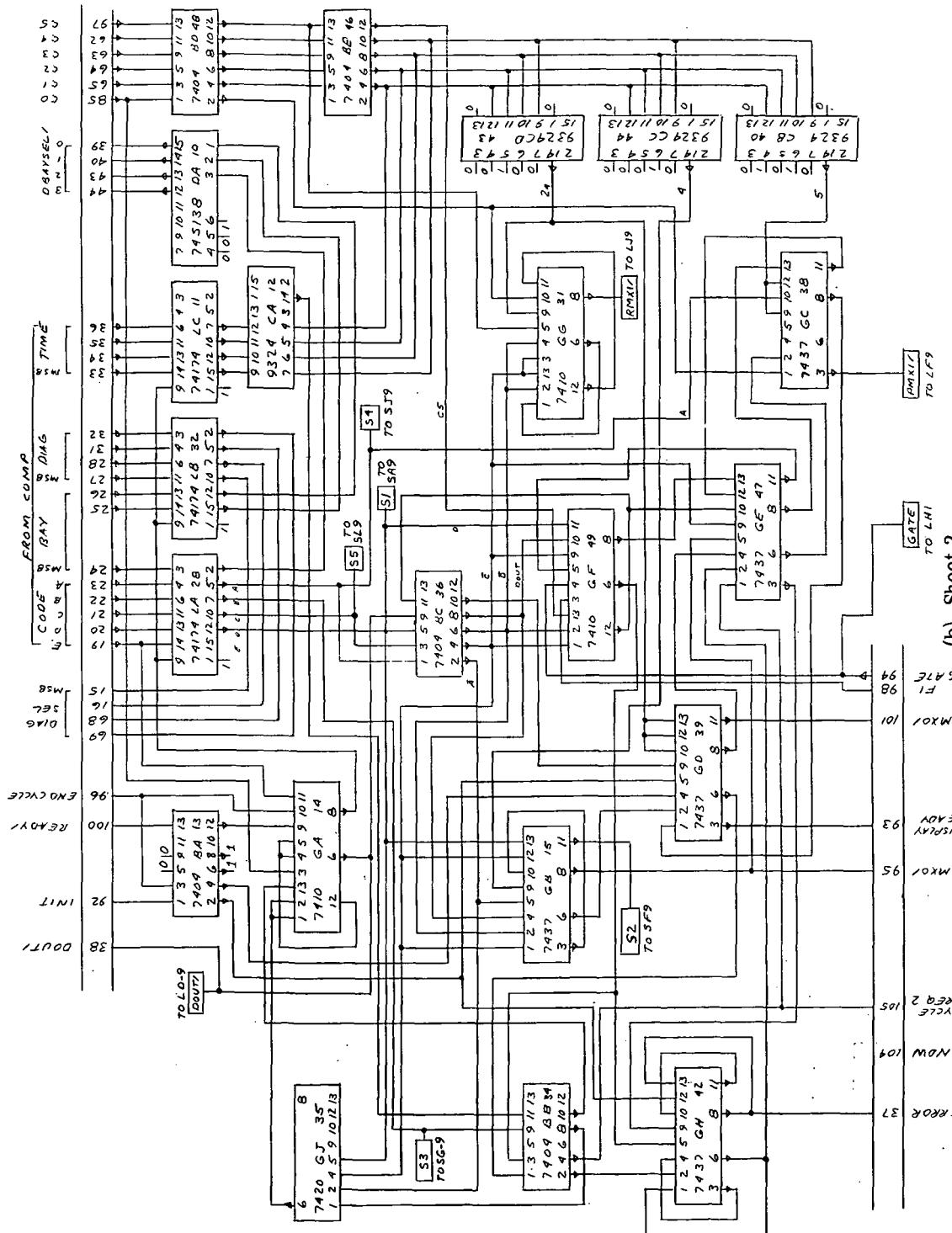
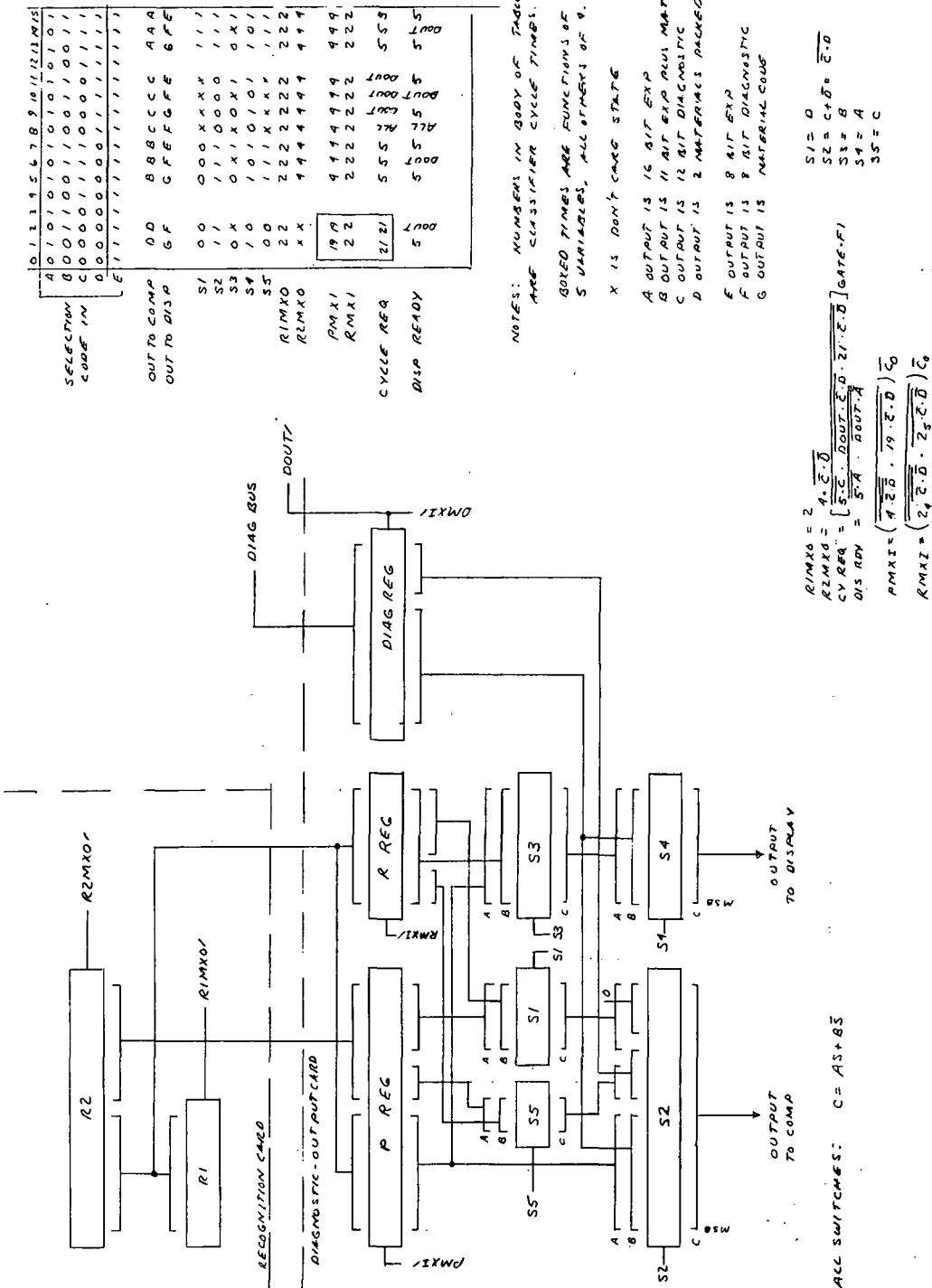


FIGURE 18. DIAGNOSTIC/OUTPUT (Continued)



FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN

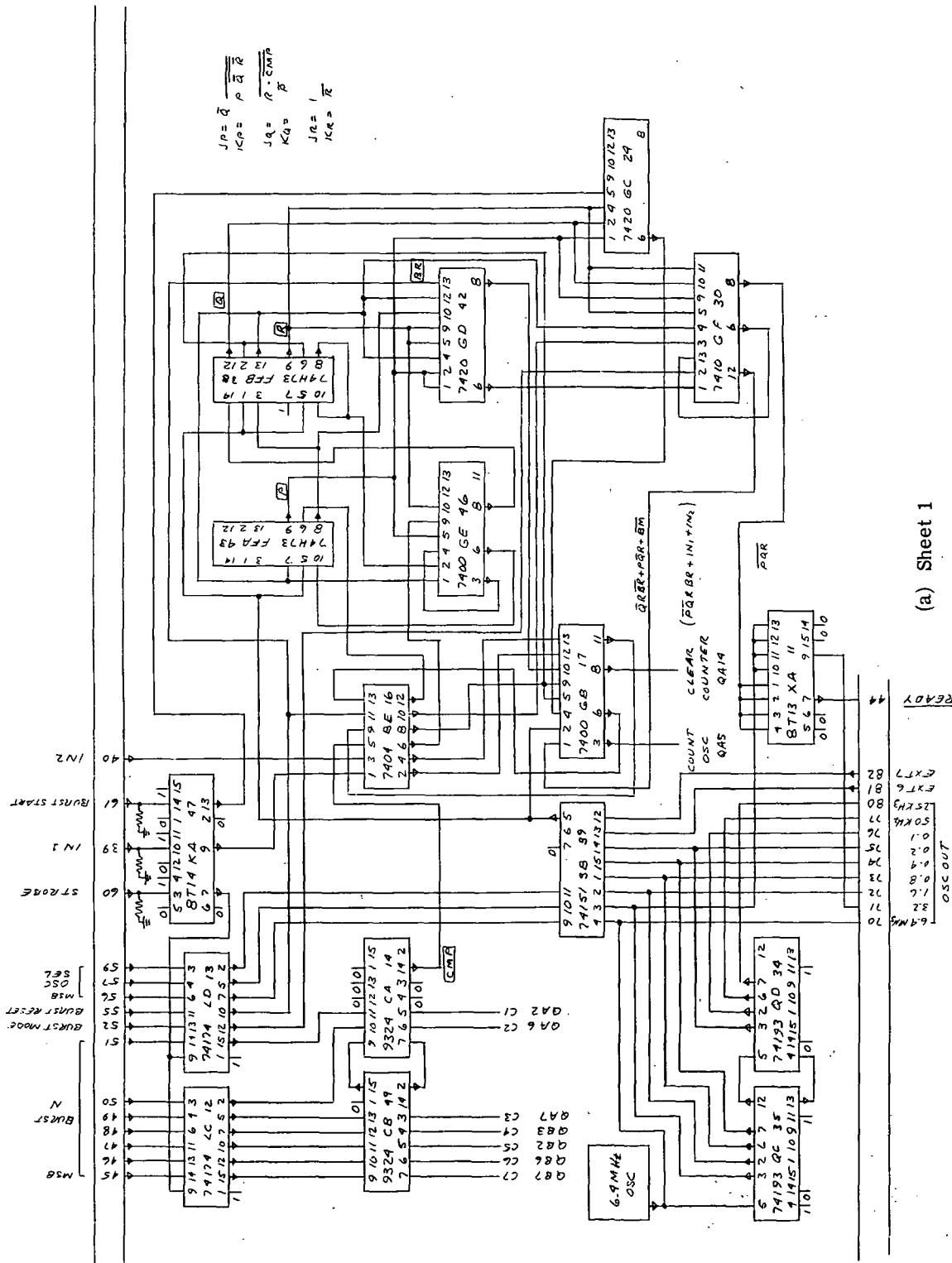


(c) Switching Diagram and Controls

FIGURE 18. DIAGNOSTIC/OUTPUT (Concluded)

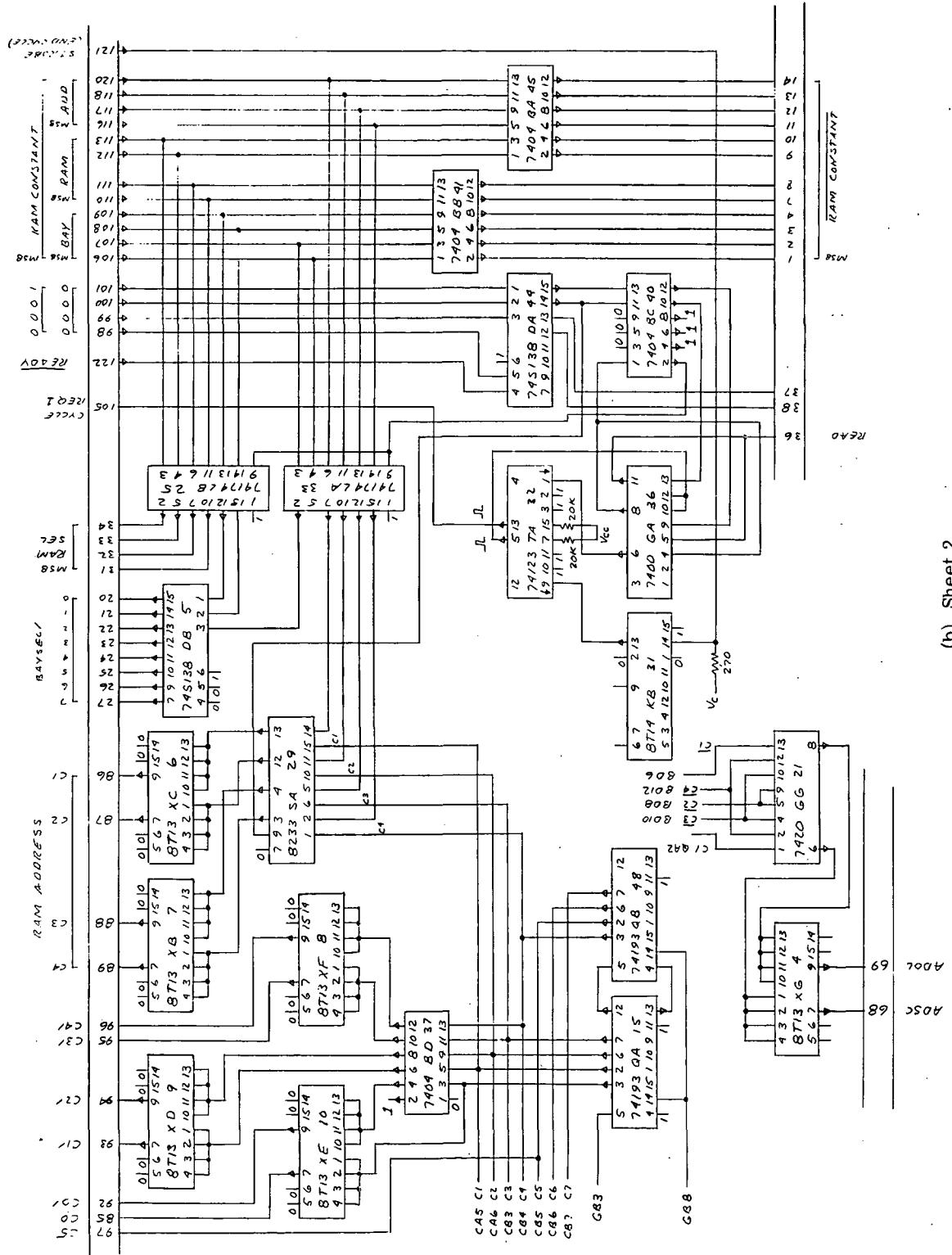


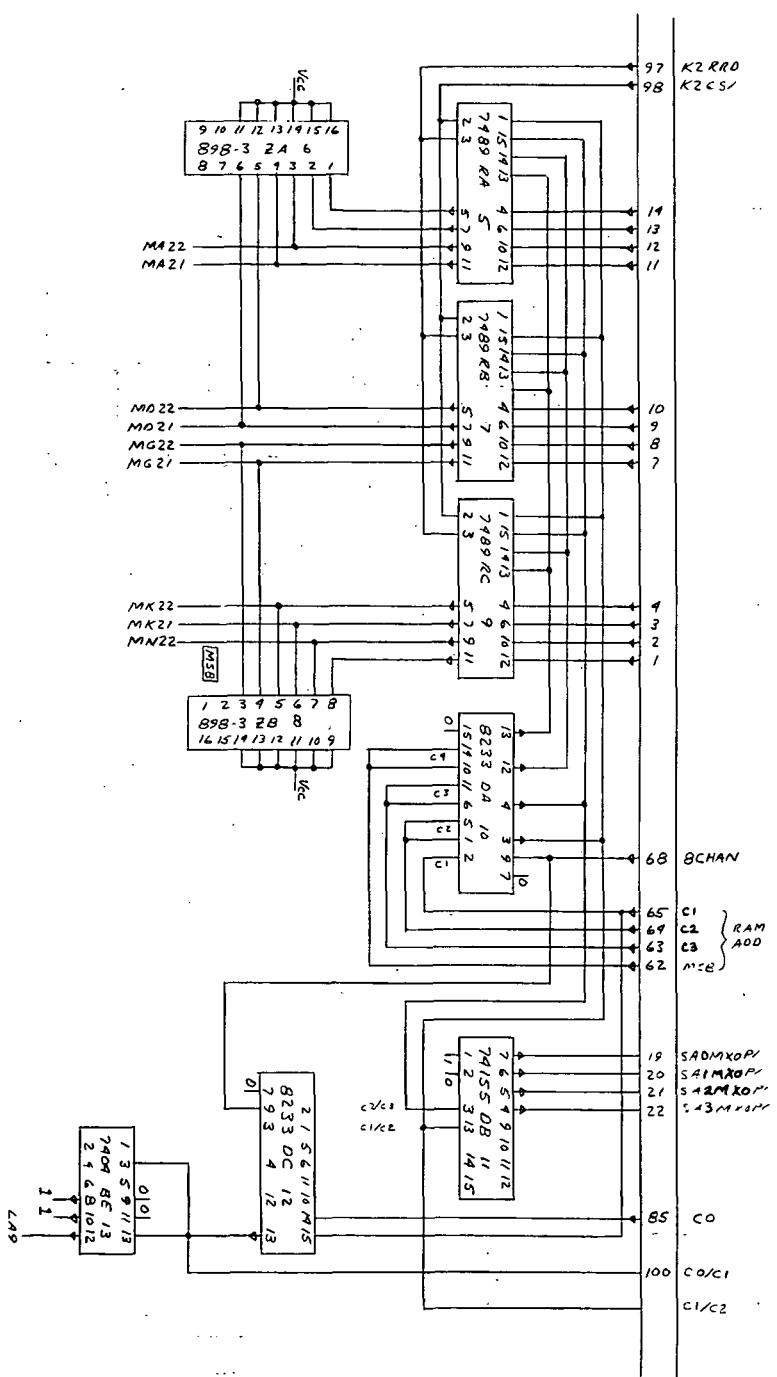
FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN



(a) Sheet 1

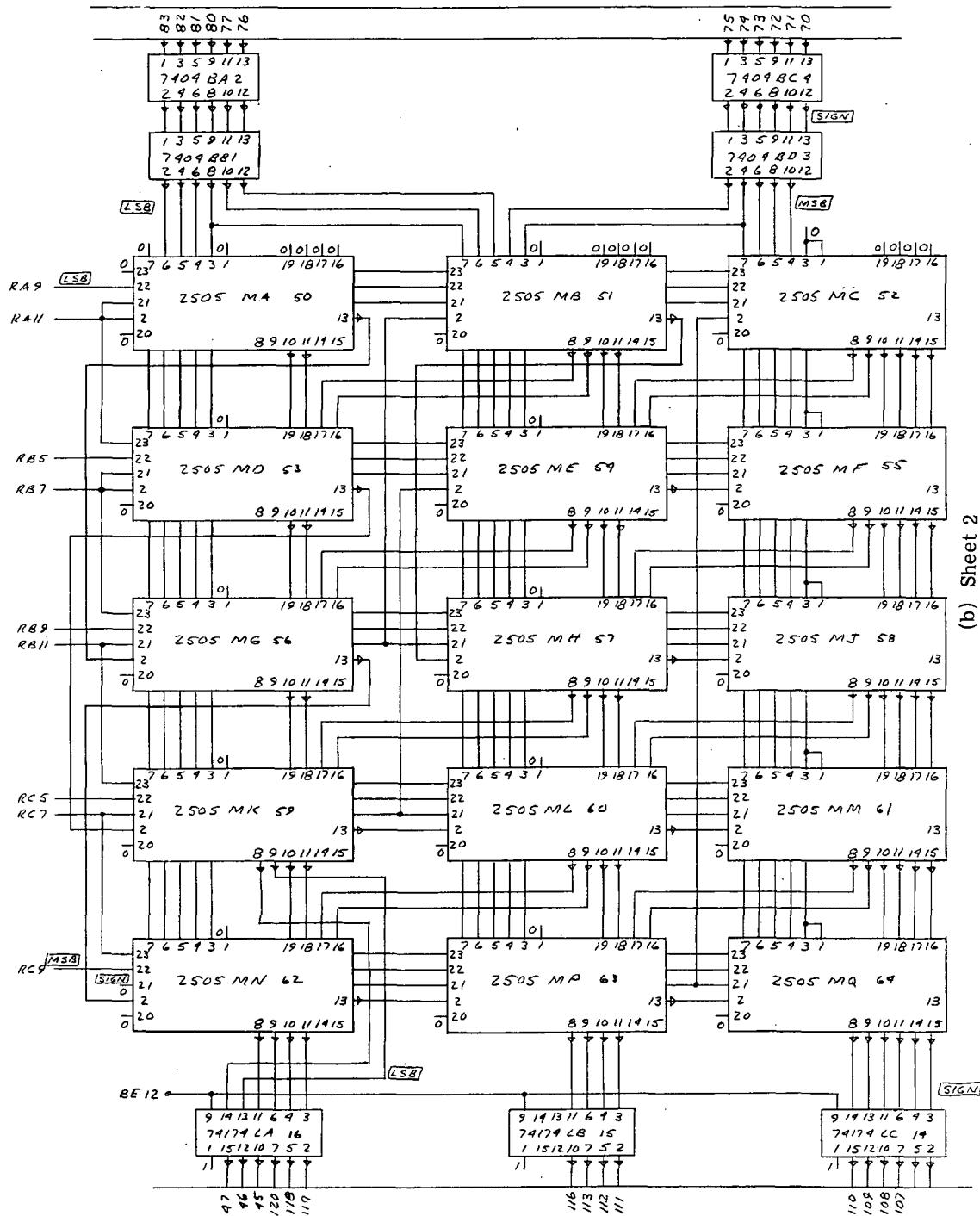
FIGURE 19. CLOCK (Continued)





(a) Sheet 1,

FIGURE 20. k^2 (Continued)



(b) Sheet 2
FIGURE 20. k^2 (Concluded)

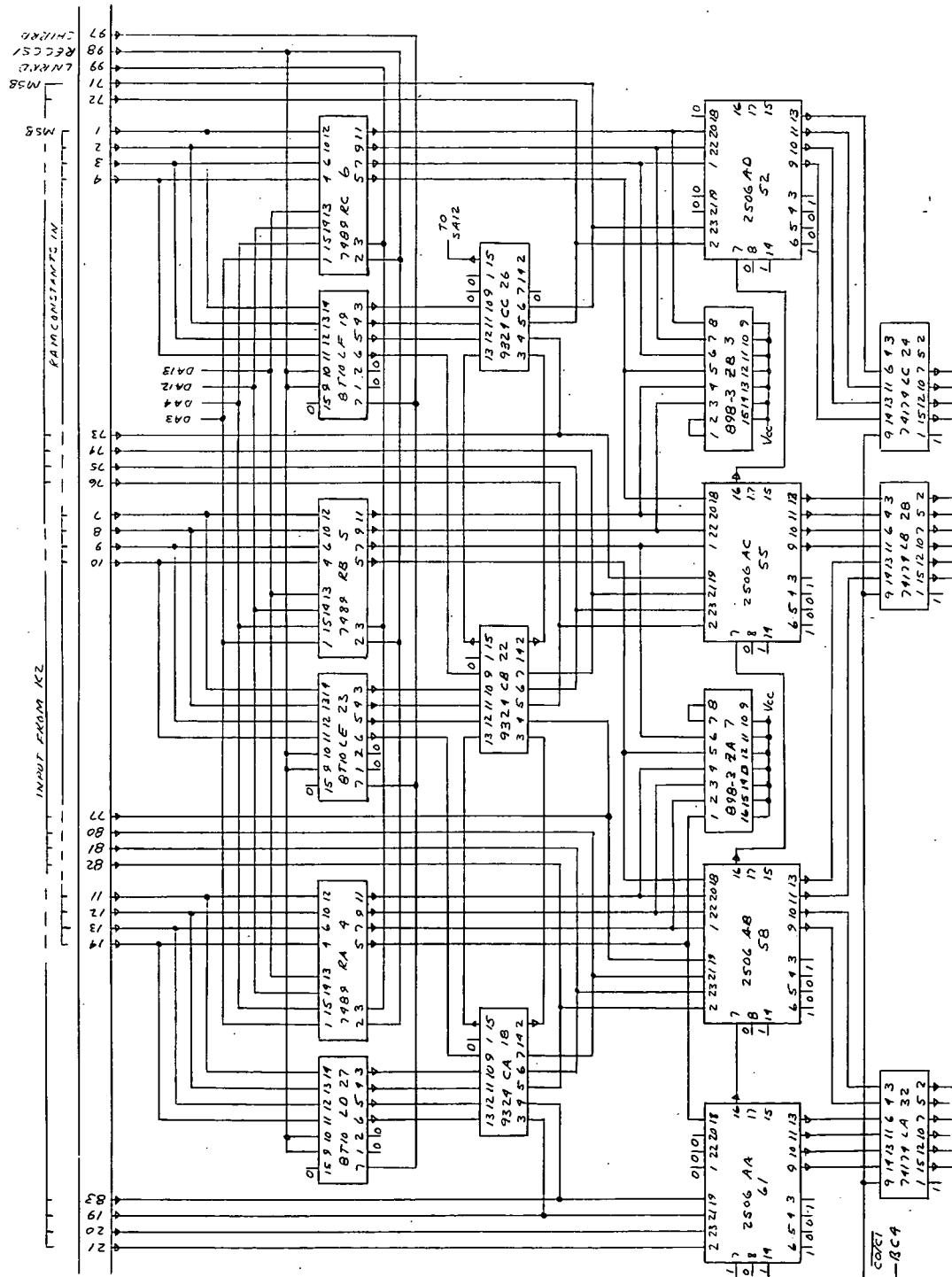


FIGURE 21. RECOGNITION (Continued)
 (a) Sheet 1



FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN

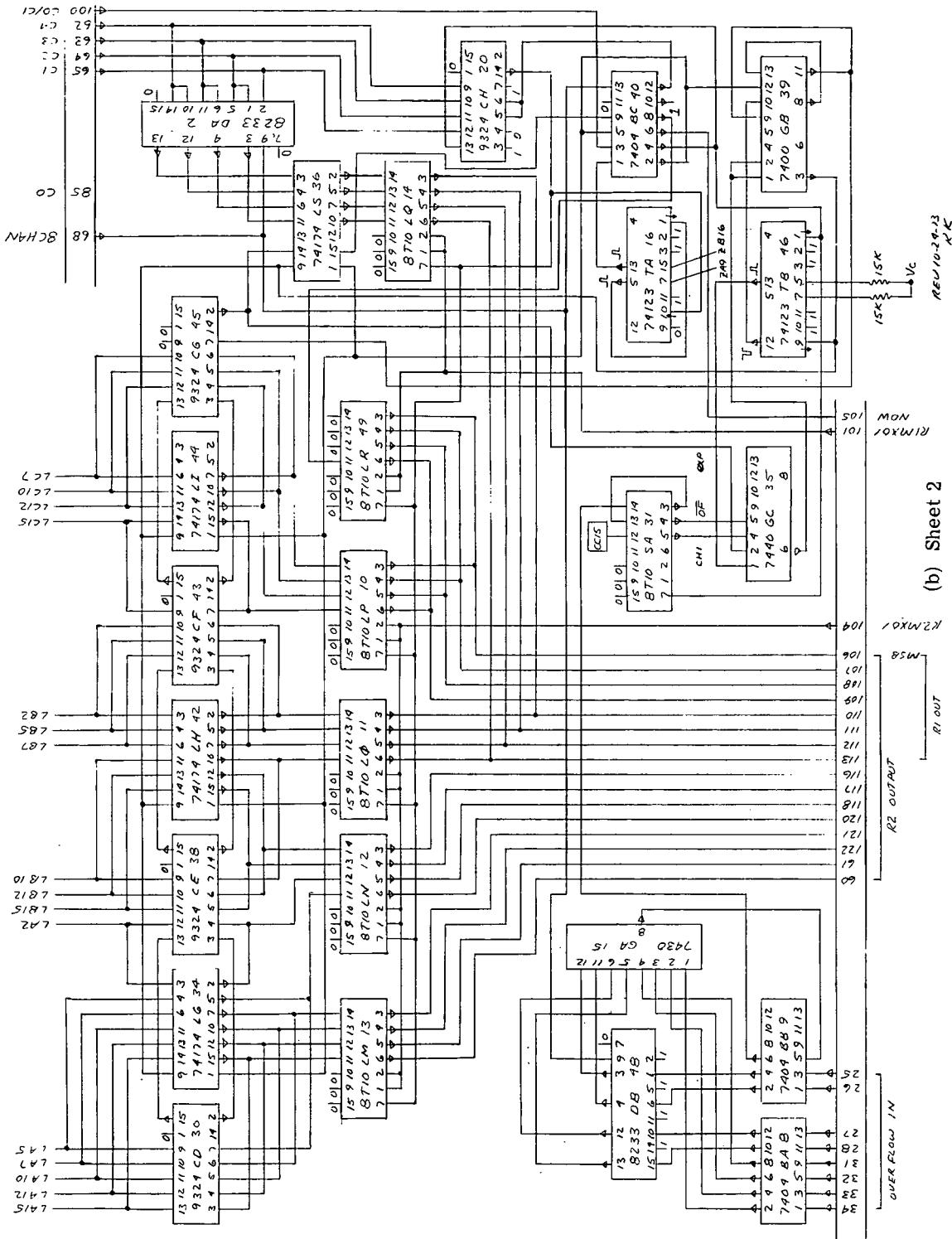


FIGURE 21. RECOGNITION (Concluded)



FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN

4

CONTROL AND HYBRID SECTION

The hybrid section of the classifier contains nineteen cards, of which sixteen are identical printed circuit cards. These cards, located in slots H-1 through H-16, perform the transfer of data to the classifier. A block diagram of the control and hybrid section is shown in Fig. 22 and a detailed block diagram of the hybrid cards is shown in Fig. 23. For a description of this classifier section, see Section 6 of Vol. I.

The transfer of data from the PDP-11/45 computer is accomplished by the circuitry shown in the block diagram of Fig. 24. The transfer of digitized data to the computer is controlled by the digital output synchronizer shown in the block diagram of Fig. 25.

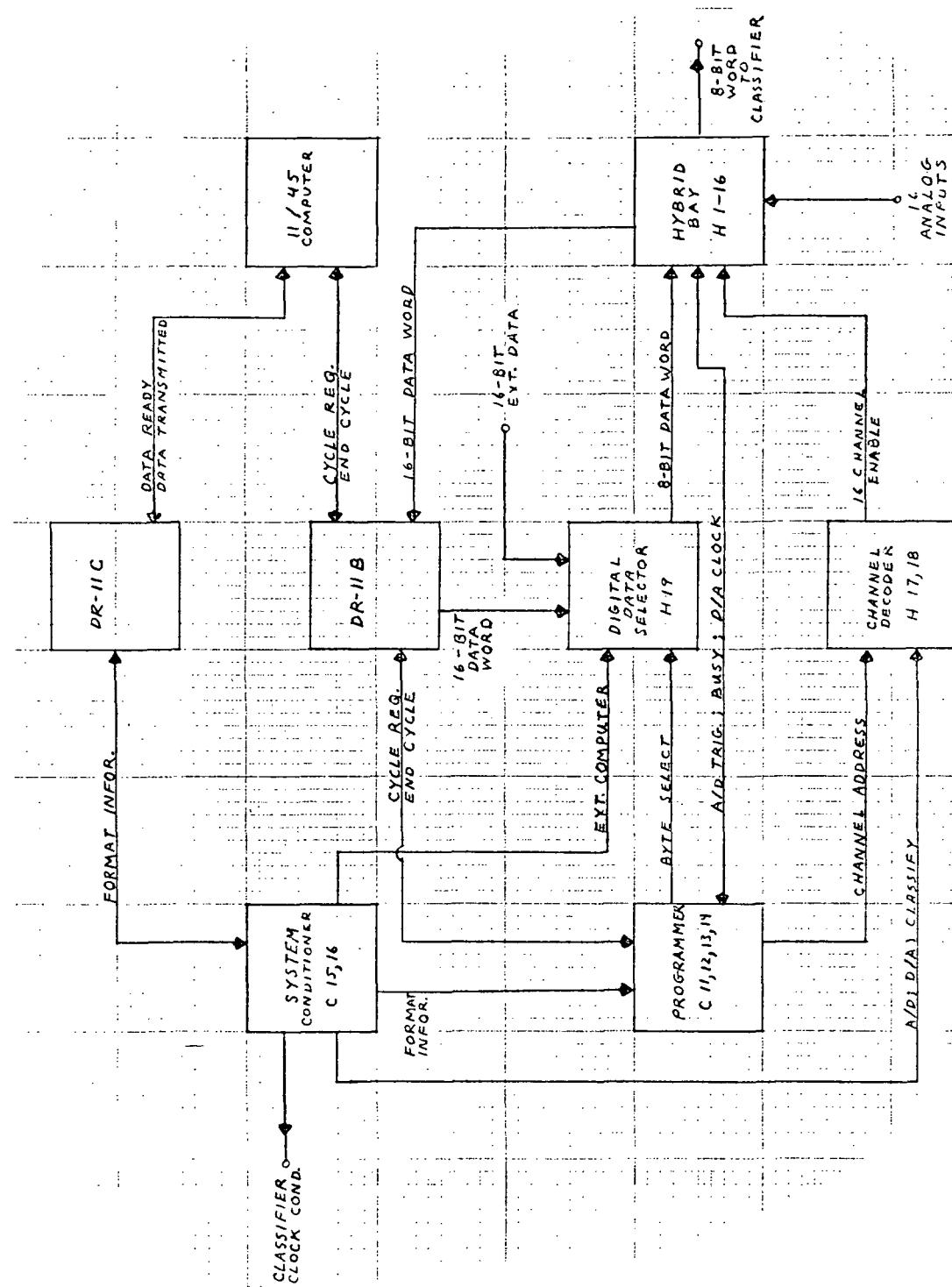


FIGURE 22. CONTROL SECTION

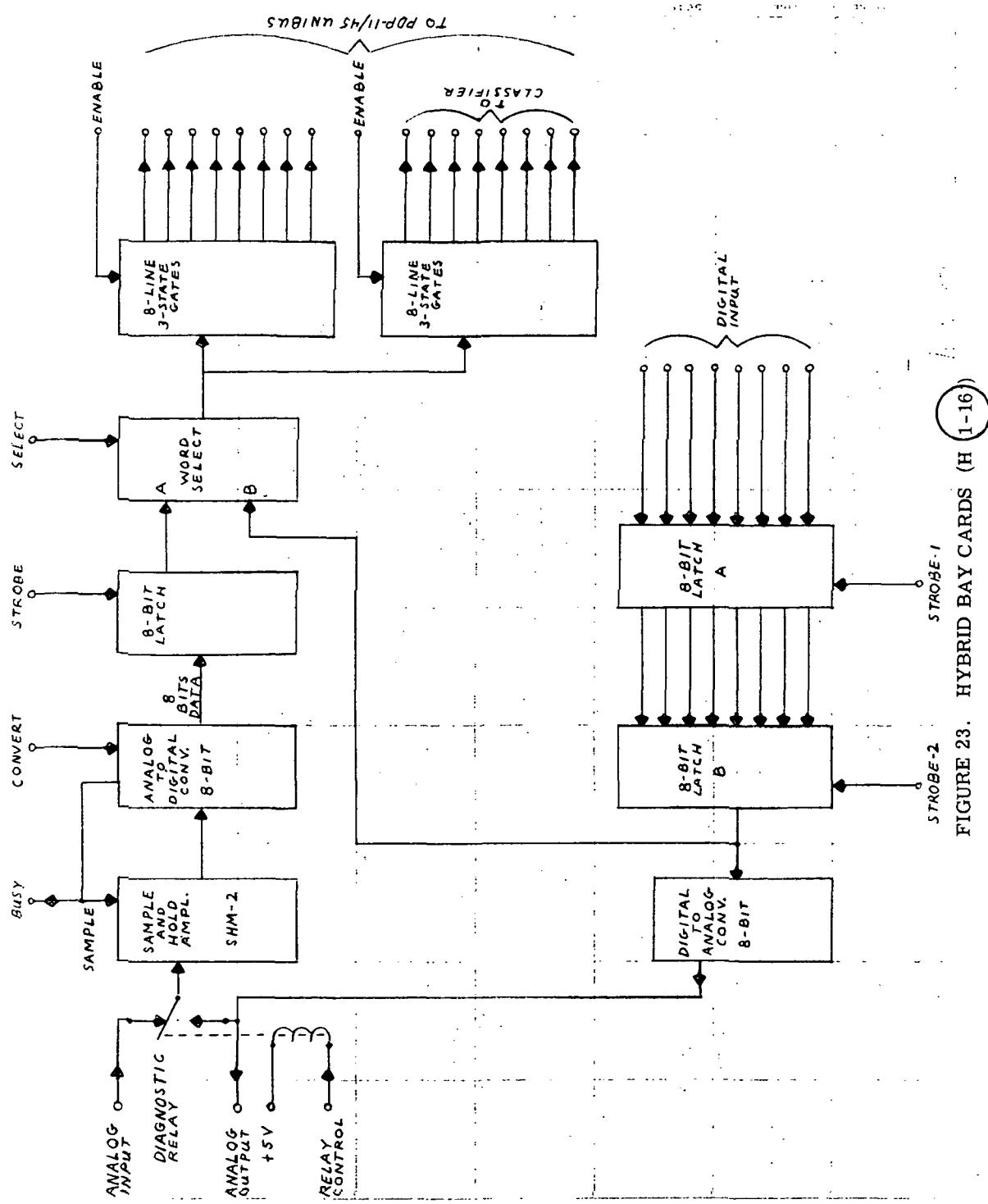


FIGURE 23. HYBRID BAY CARDS (H 1-16)

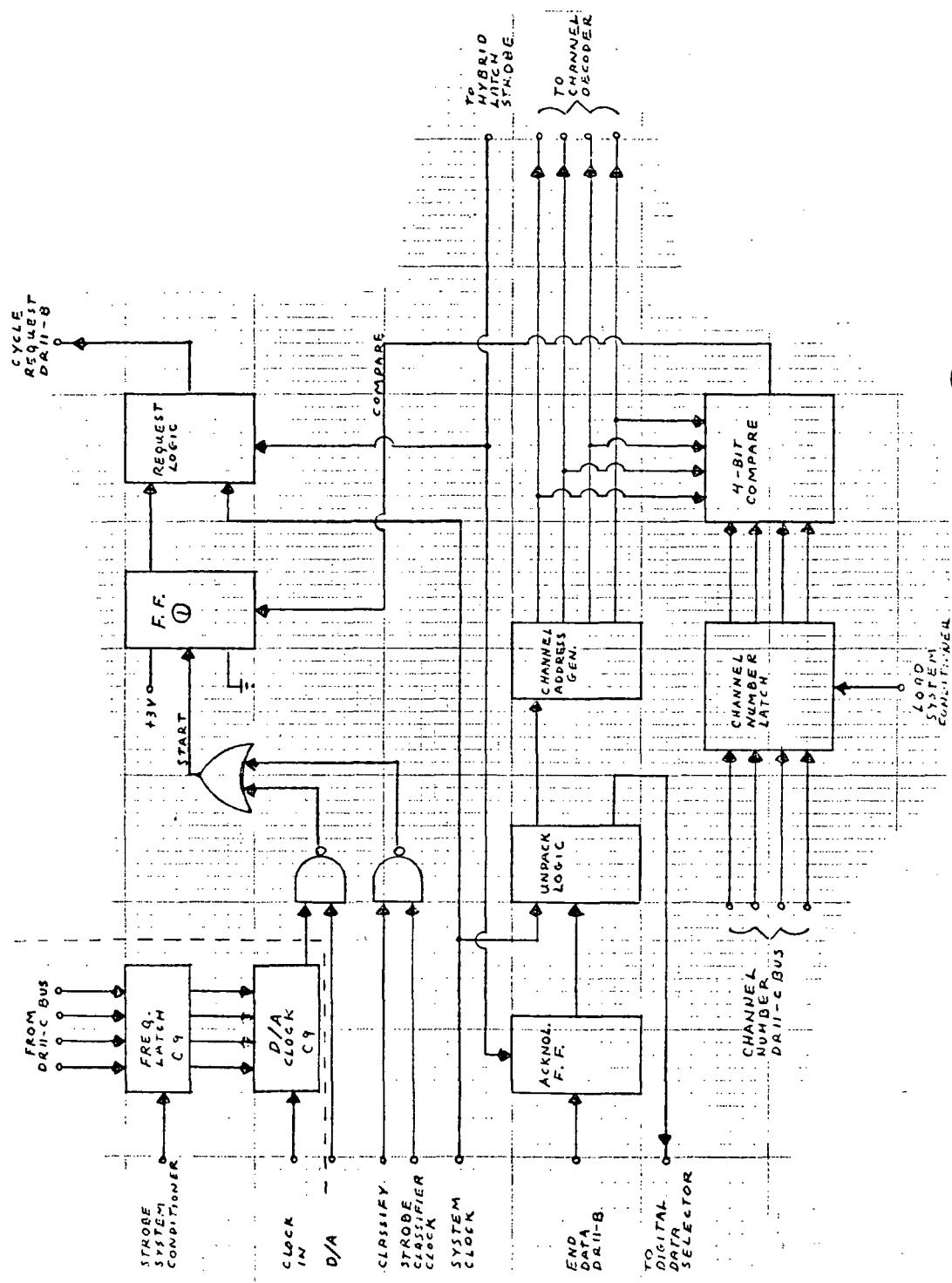


FIGURE 24. DIGITAL INPUT SYNCHRONIZER (C 11,12)

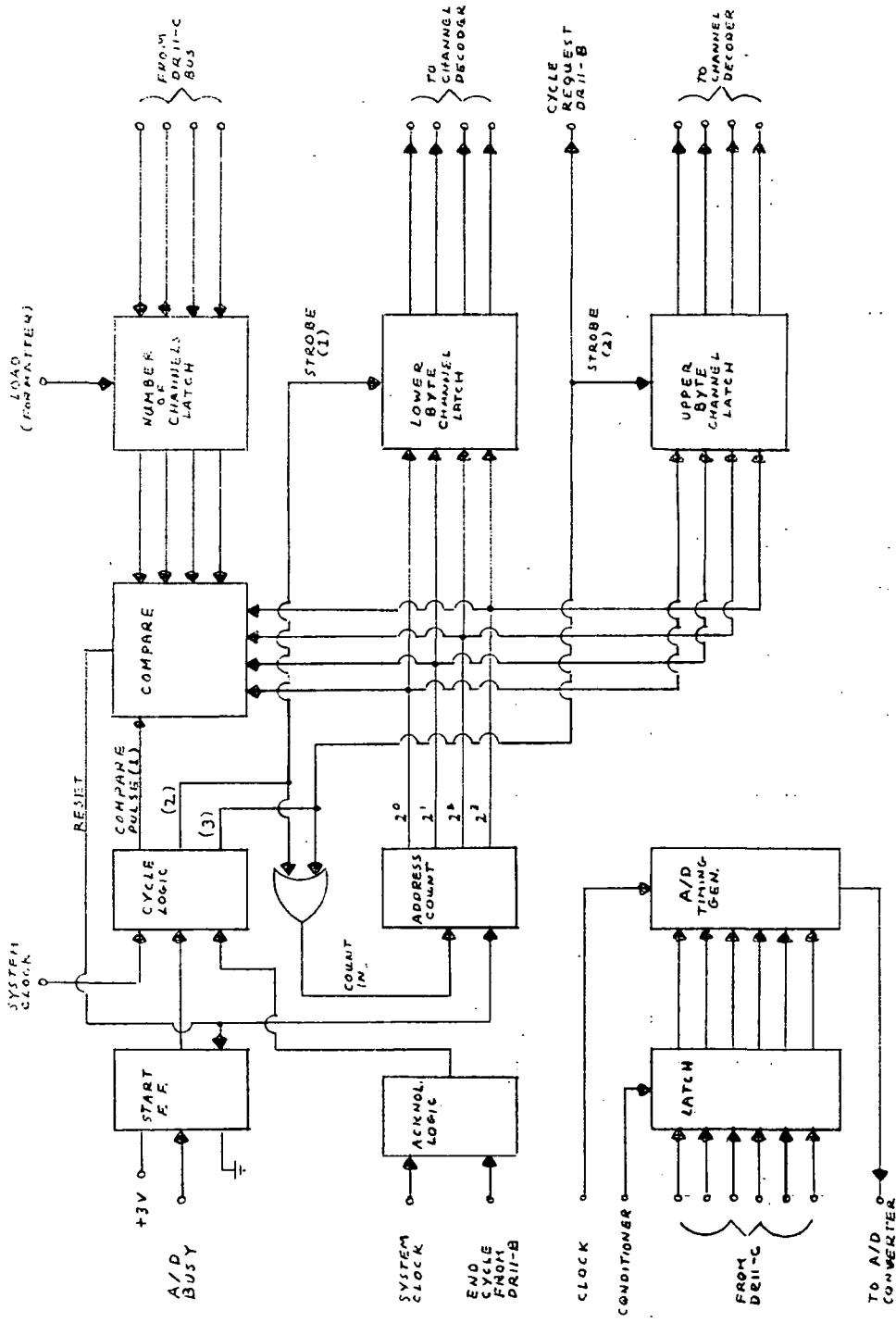


FIGURE 25. DIGITAL OUTPUT SYNCHRONIZER (C 13,14)

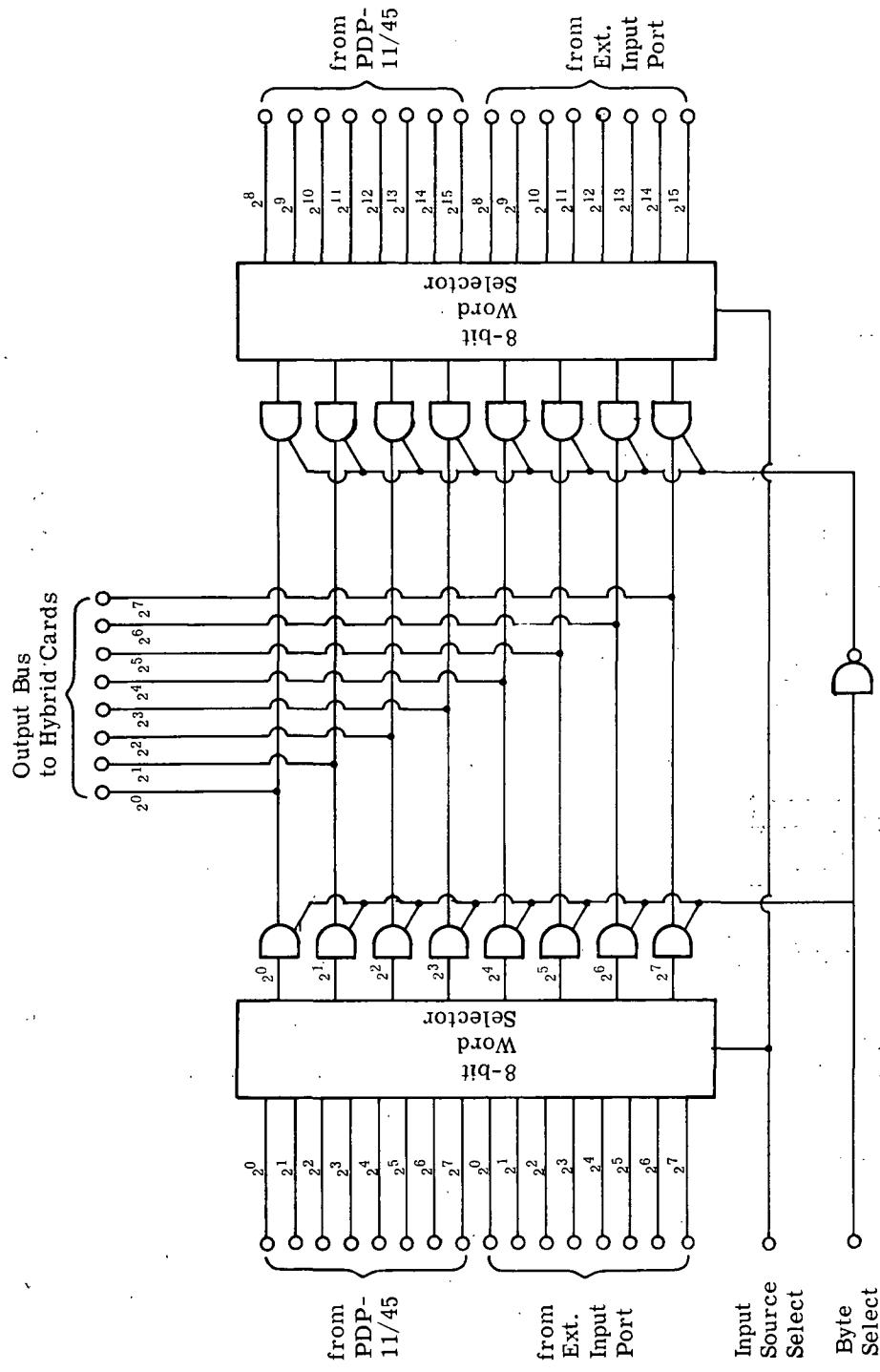


FIGURE 26. DIGITAL DATA SELECTOR (H ⑯)

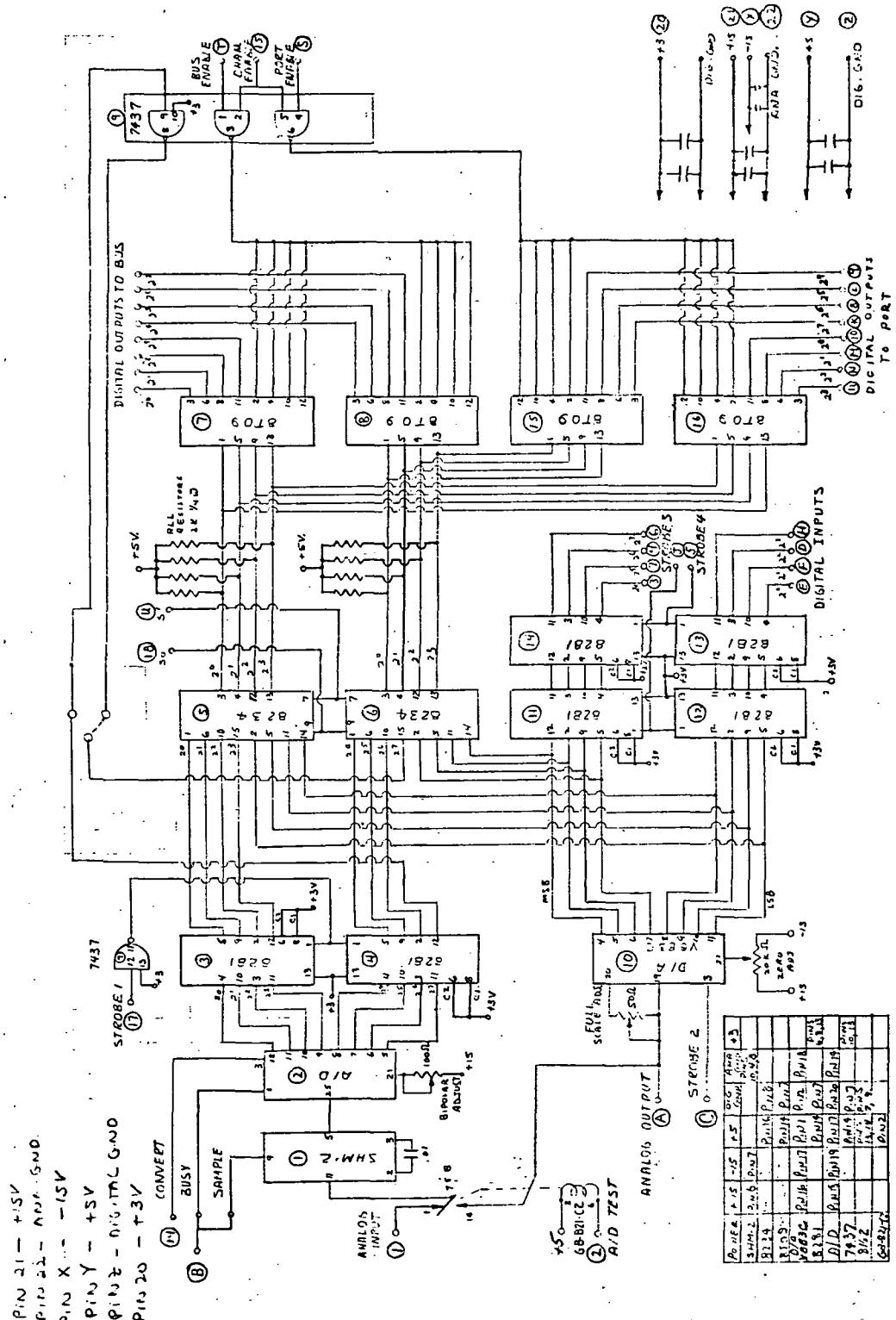


FIGURE 27. HYBRID CARDS (H 1-16)

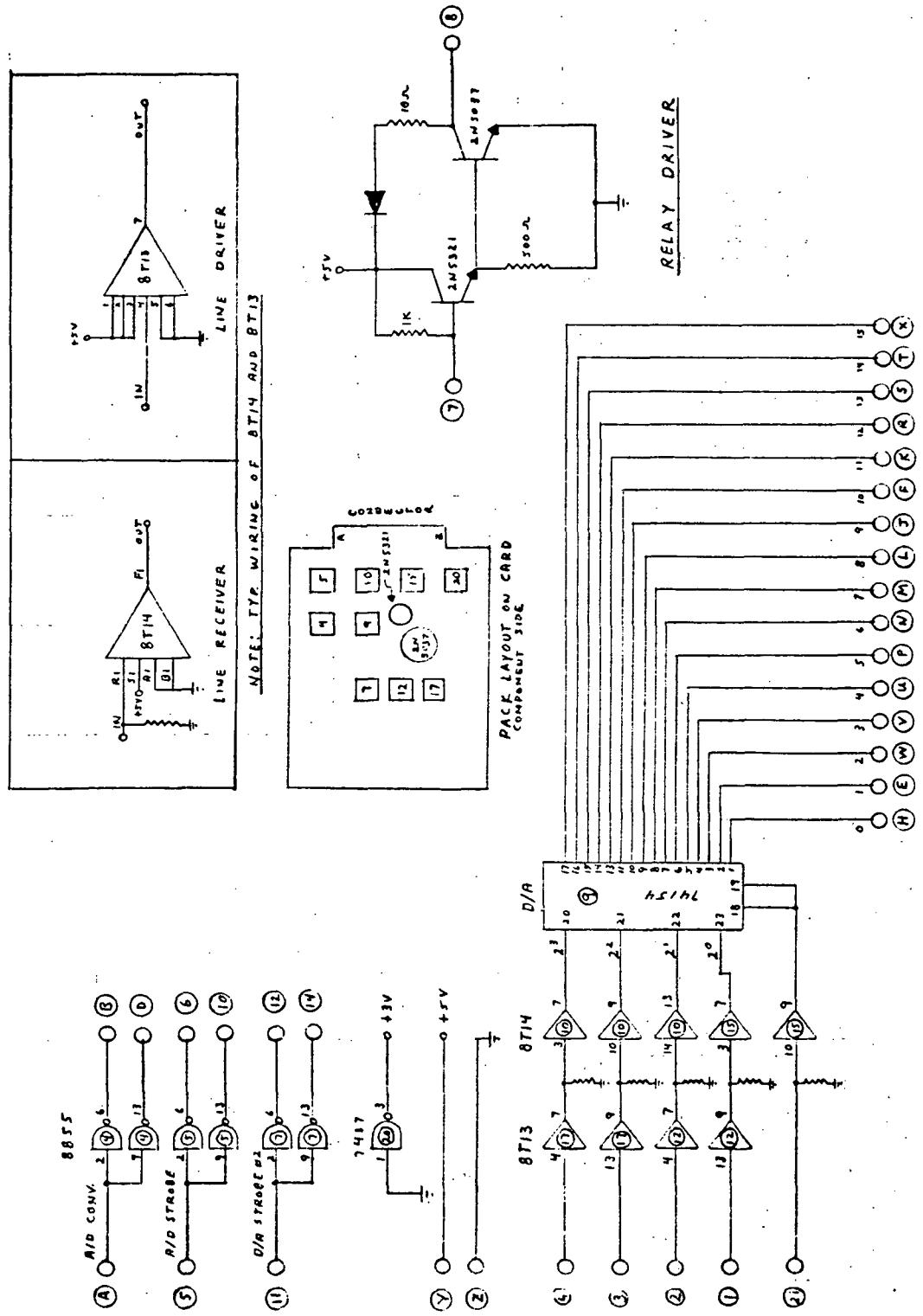


FIGURE 28. INPUT BUS AND PORT DECODER (H ⑩)

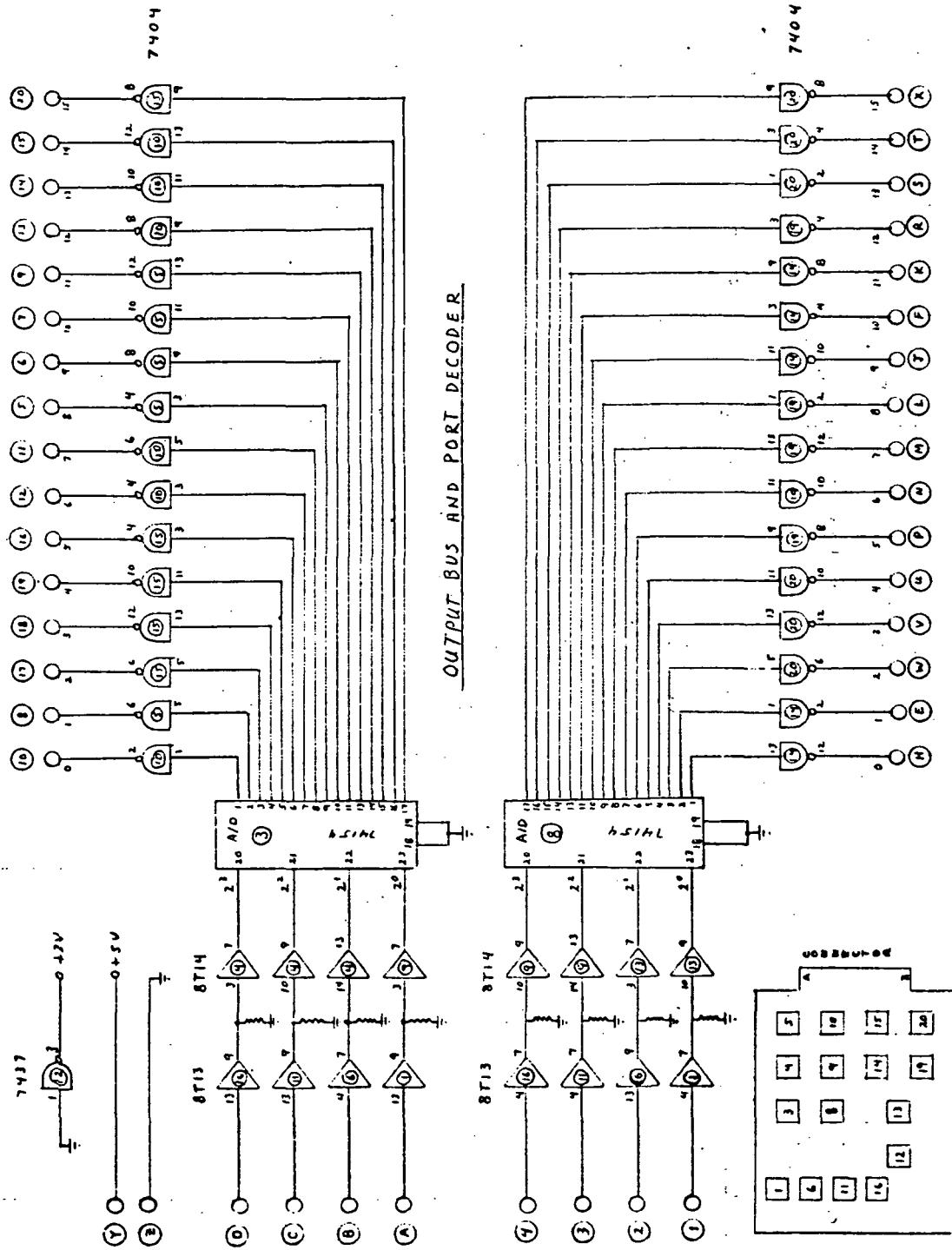


FIGURE 29. OUTPUT BUS AND PORT DECODER (H18)

PACK LAYOUT ON CARD
COMBINE PAGES 10 & 11

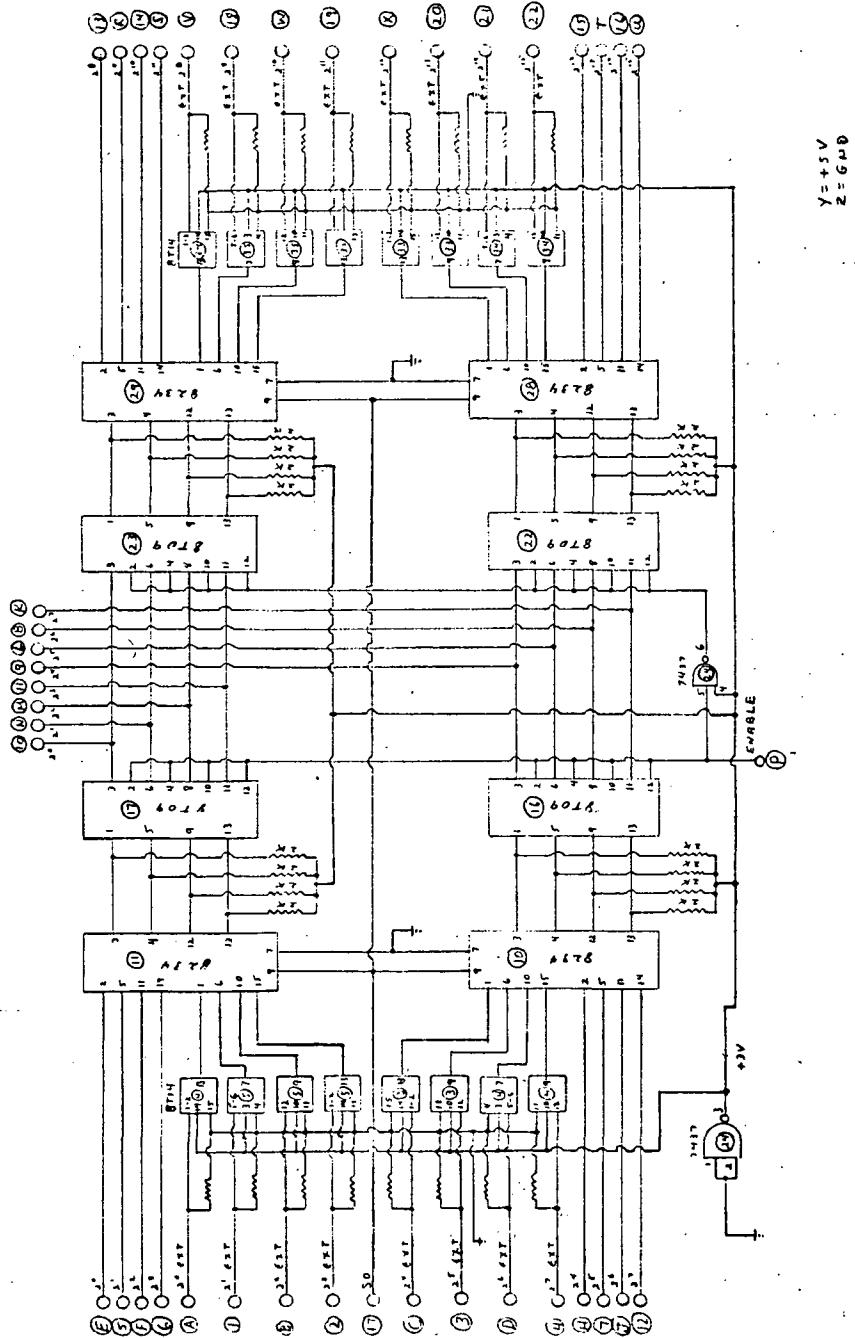


FIGURE 30. DIGITAL DATA SELECTOR (H 19)

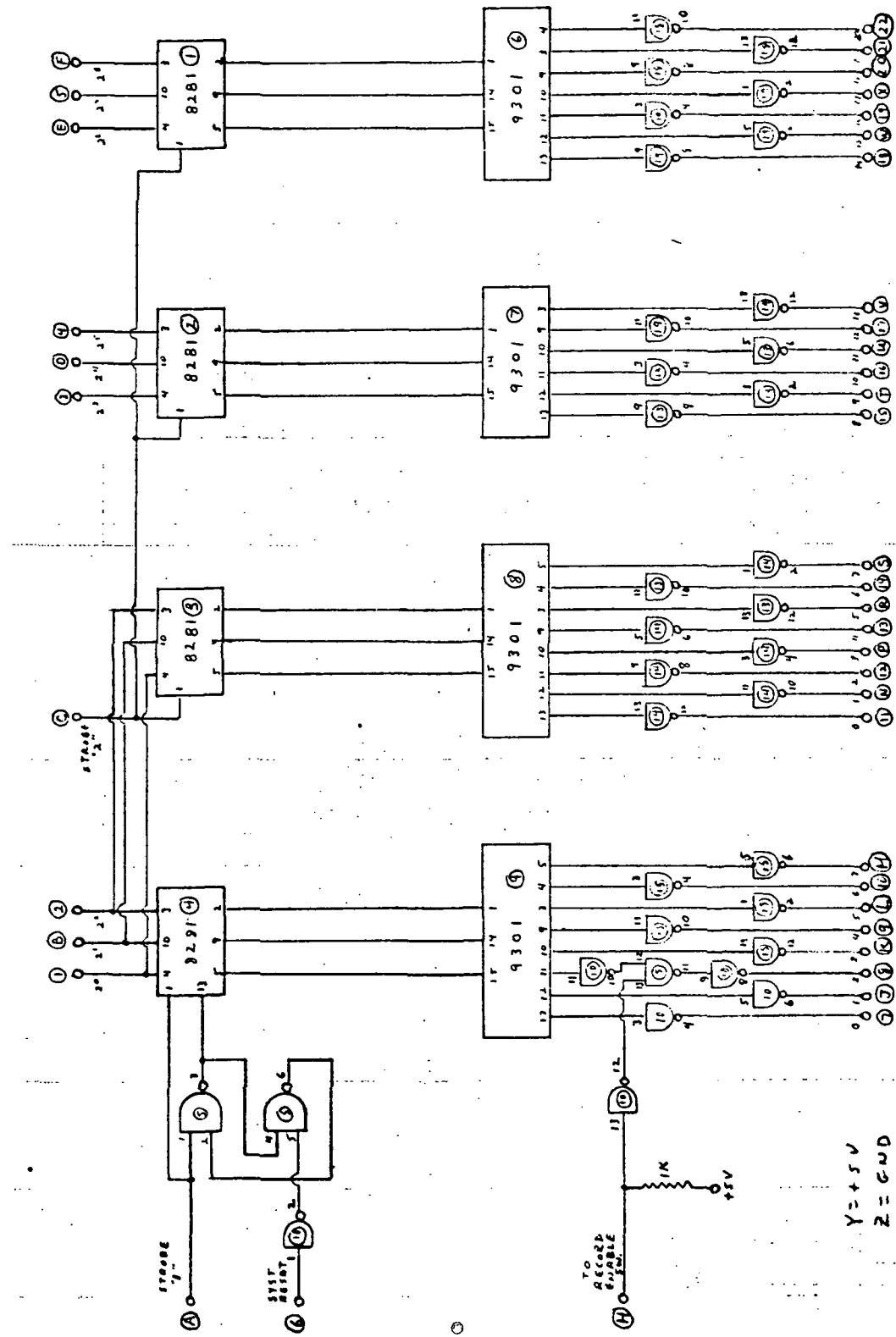


FIGURE 31. ANALOG TAPE RECORDER CONTROL (C①)

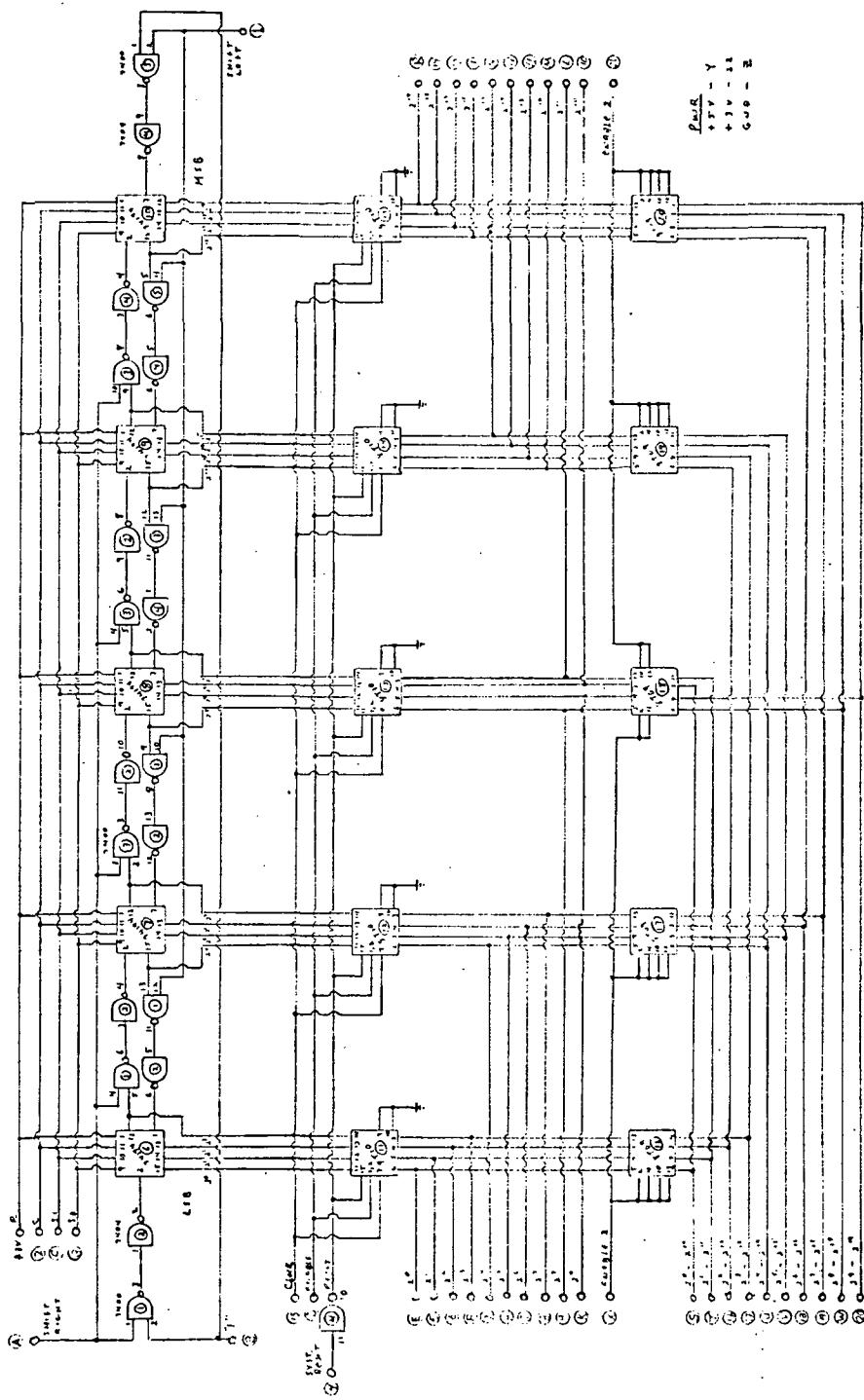


FIGURE 32. ANALOG LINE-COUNT DECODER (C②)

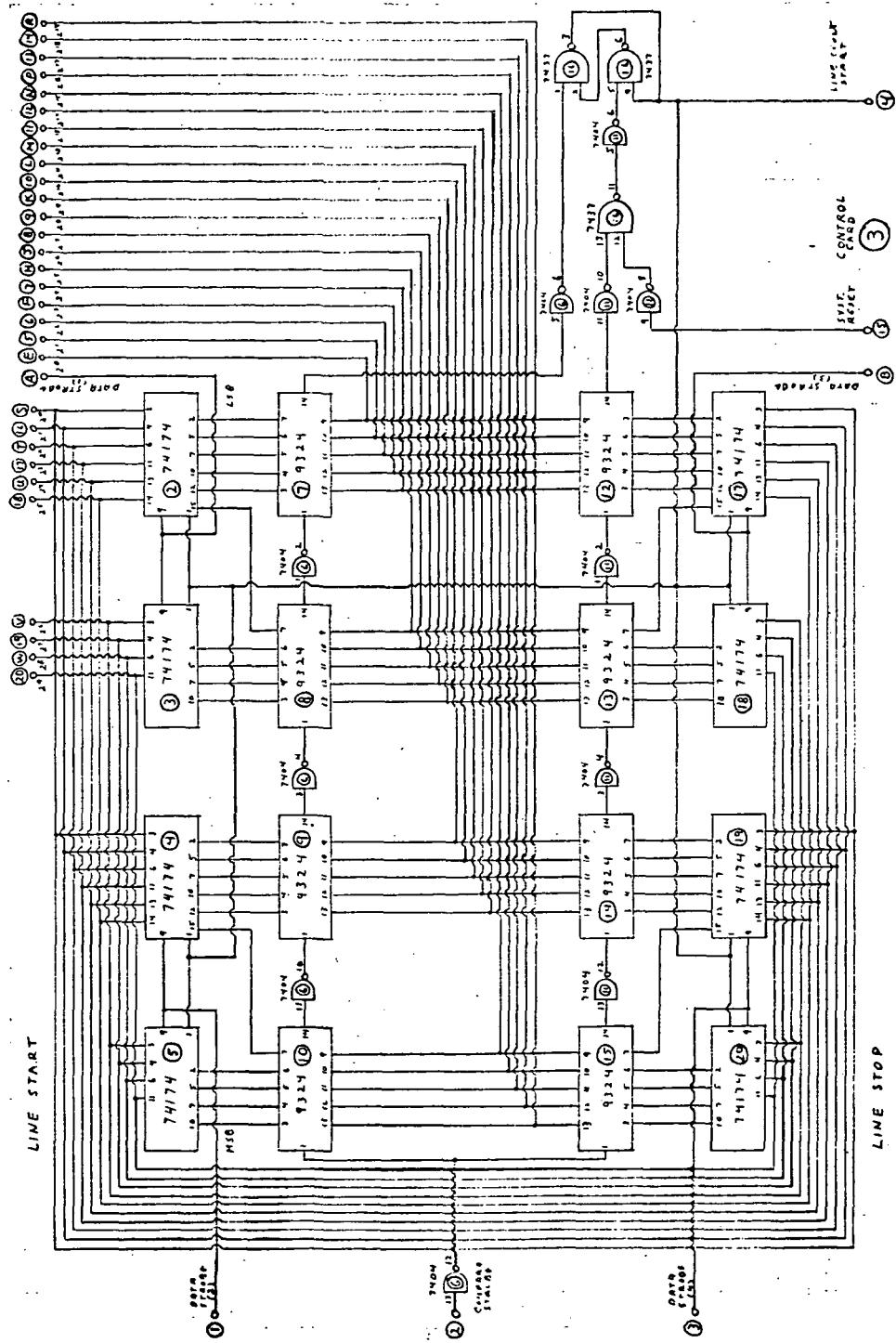


FIGURE 33. LINE-COUNT START/STOP (C ③)

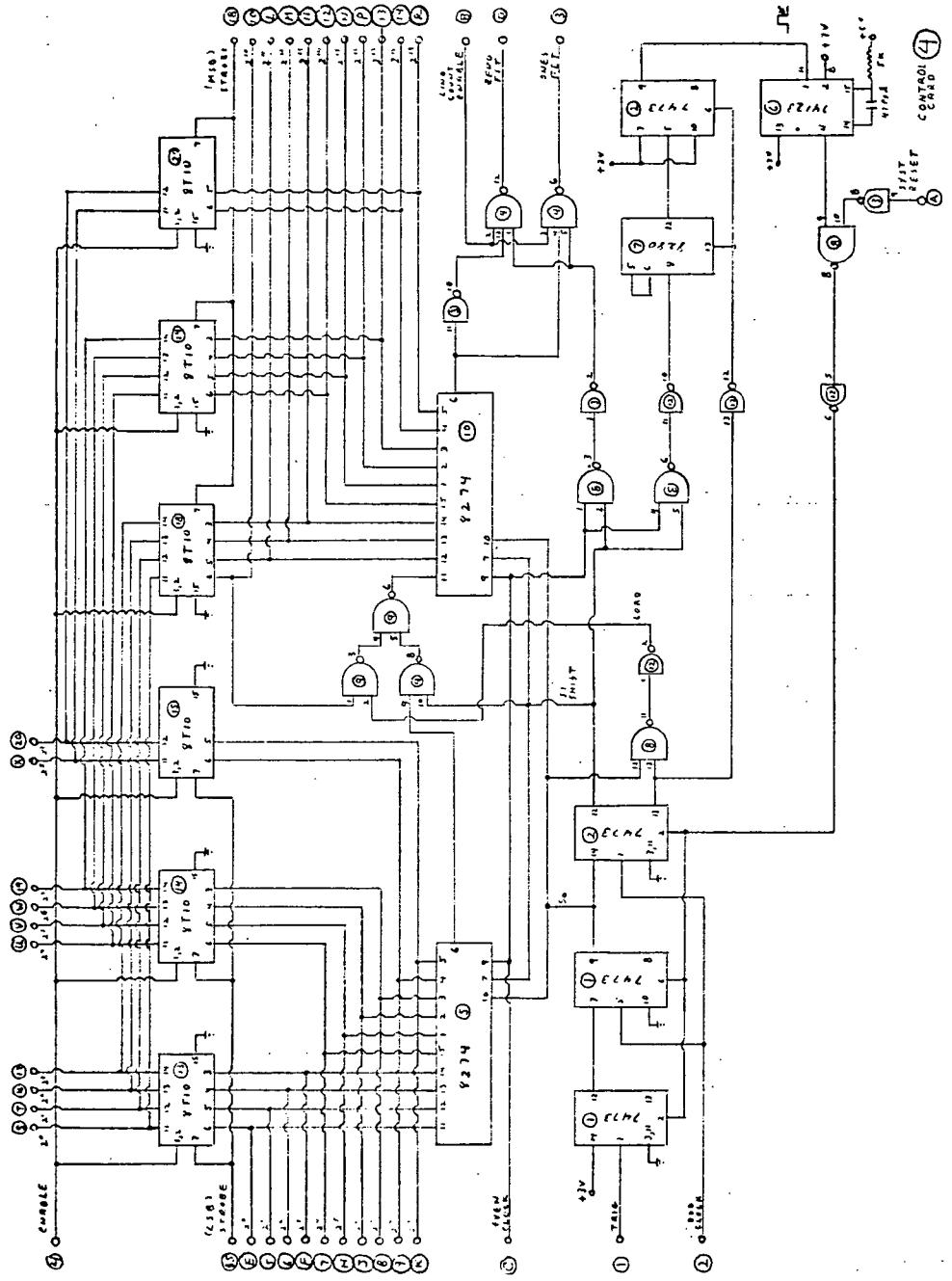


FIGURE 34. DIGITAL LINE-COUNT DECODER (C ④)

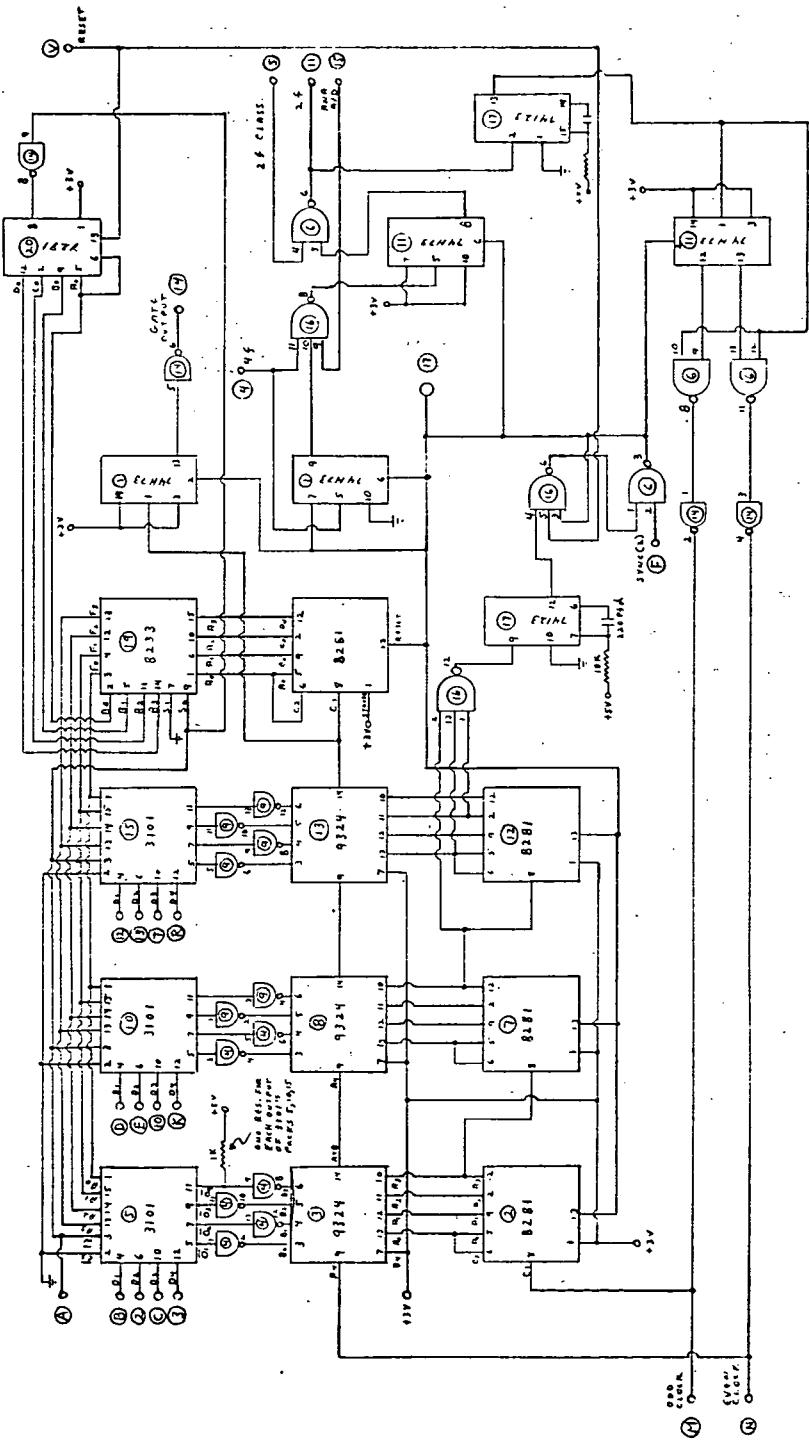


FIGURE 35. VIDEO AND CALIBRATION GENERATOR (C 6,7)

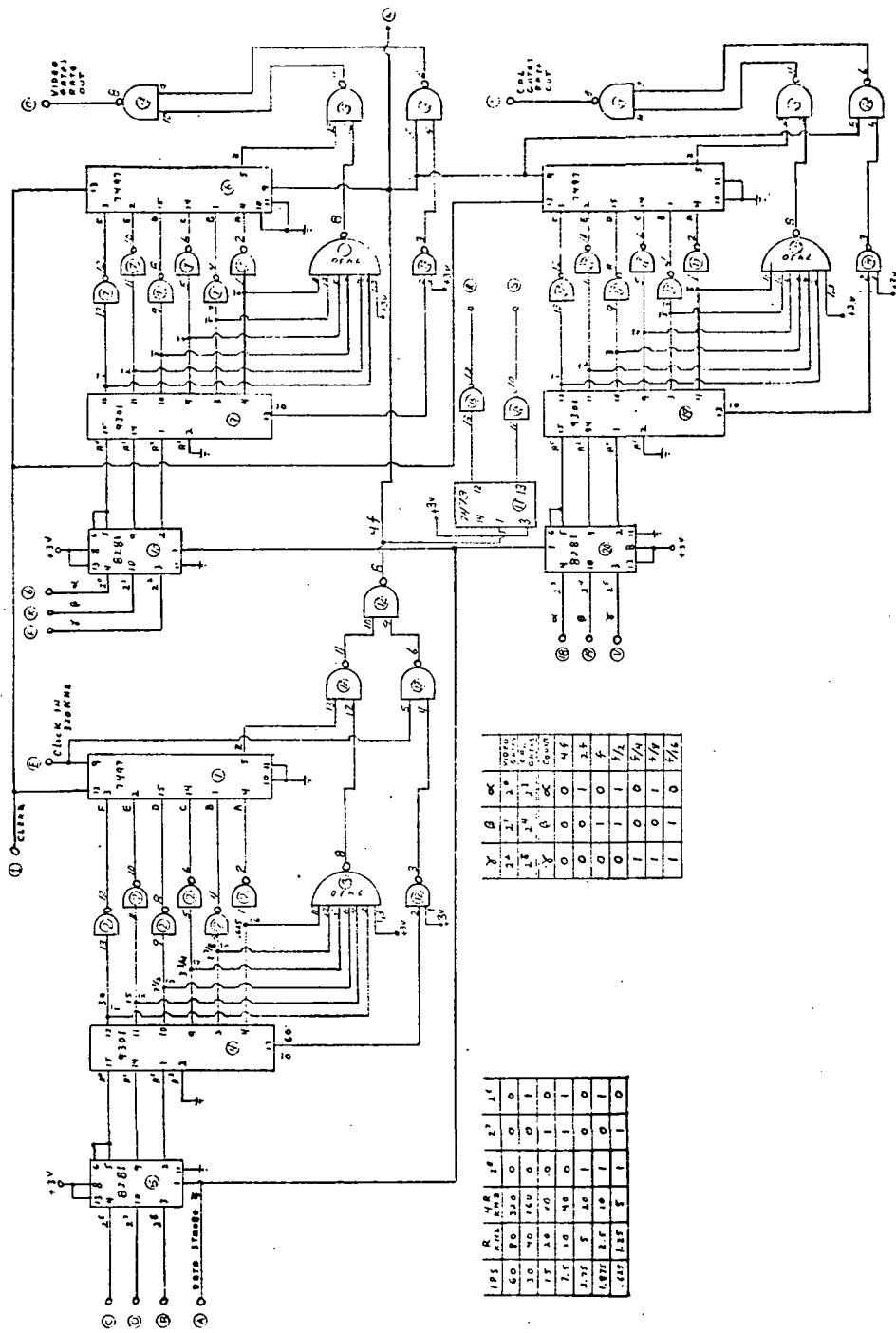


FIGURE 36. A/D-D/A CLOCK GENERATOR (C⑧)

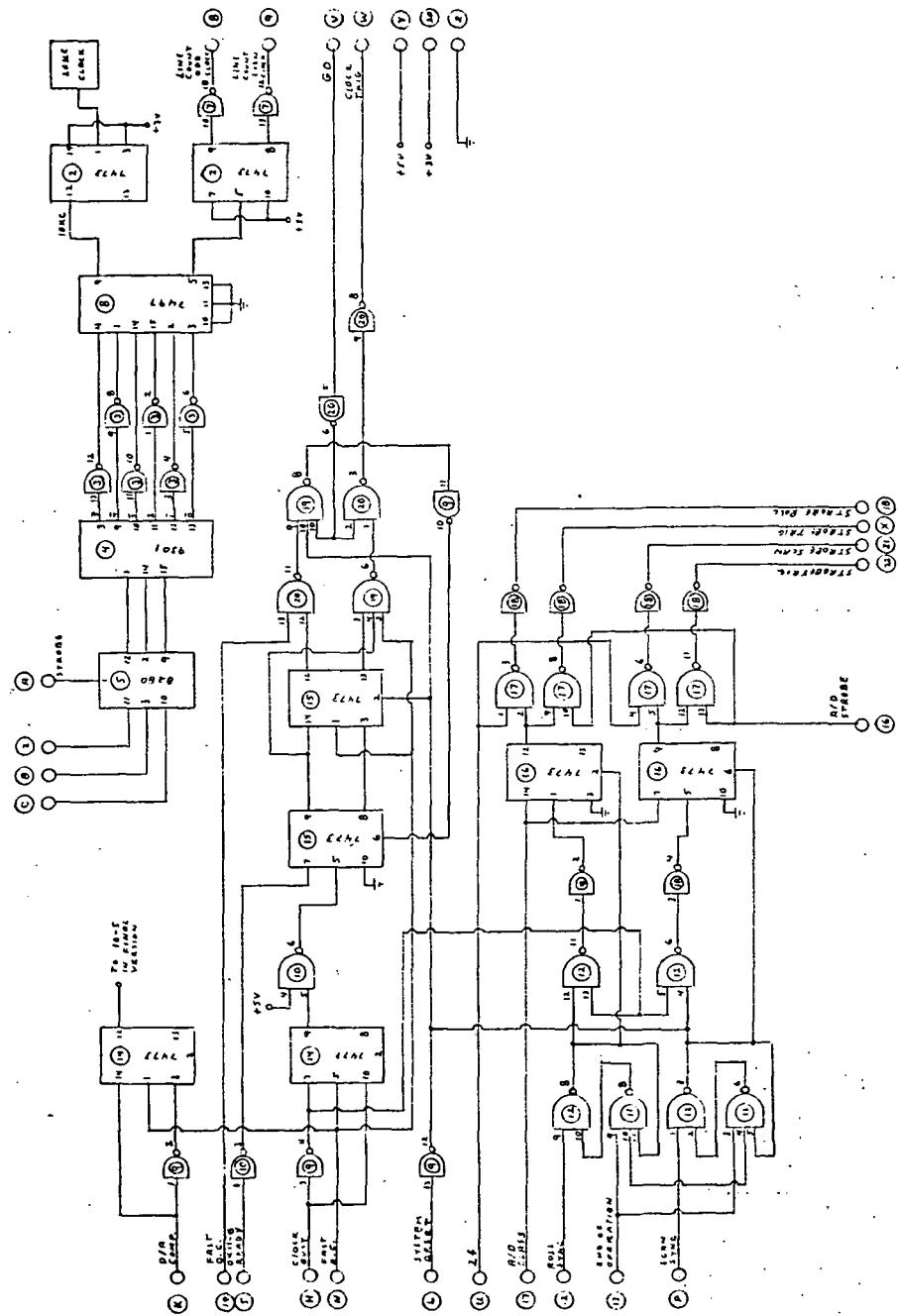


FIGURE 37. D/A LINE-COUNT CLOCK (C⑨)



FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN

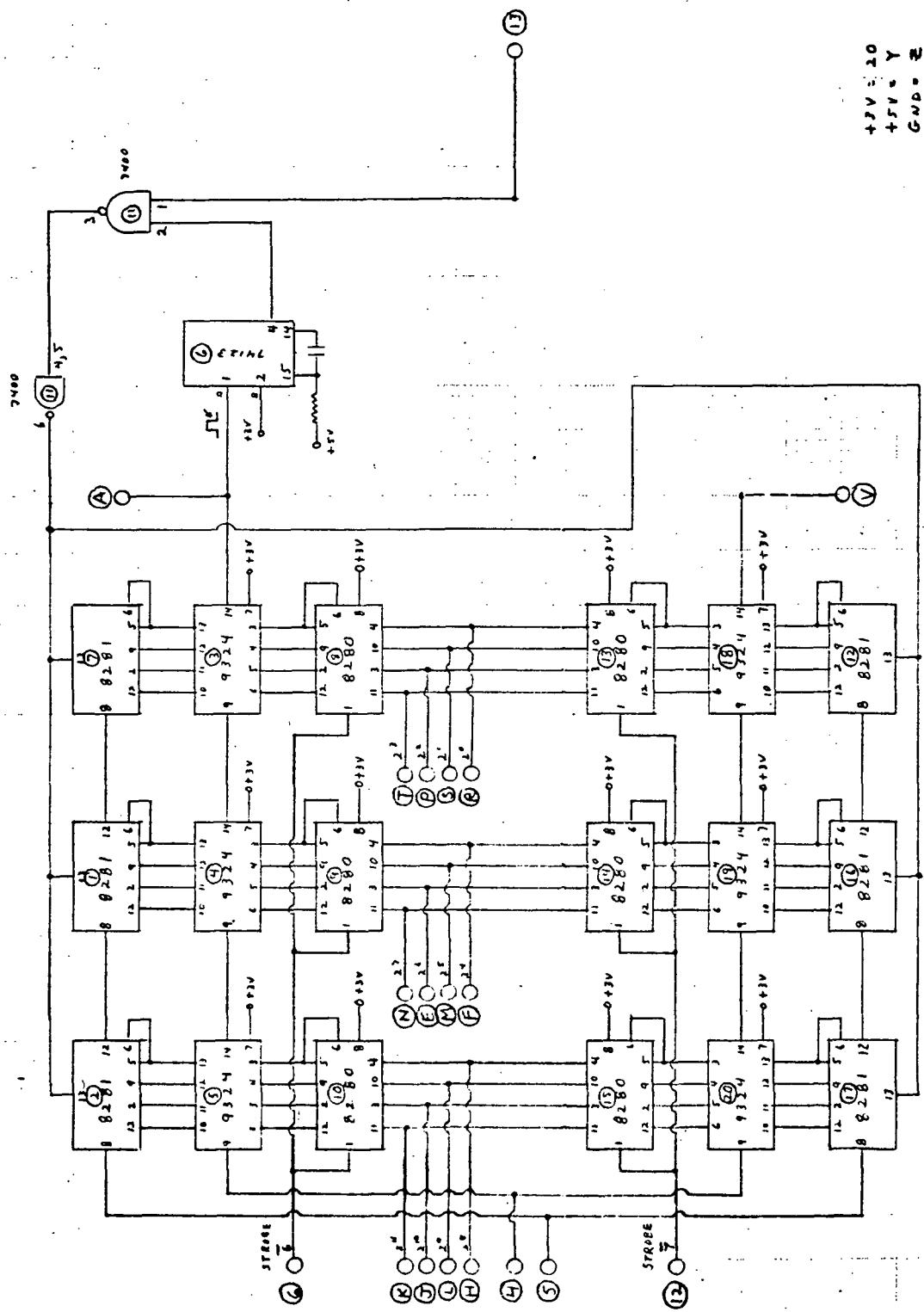


FIGURE 38. D/A DUTY CYCLE GENERATOR (C 10)

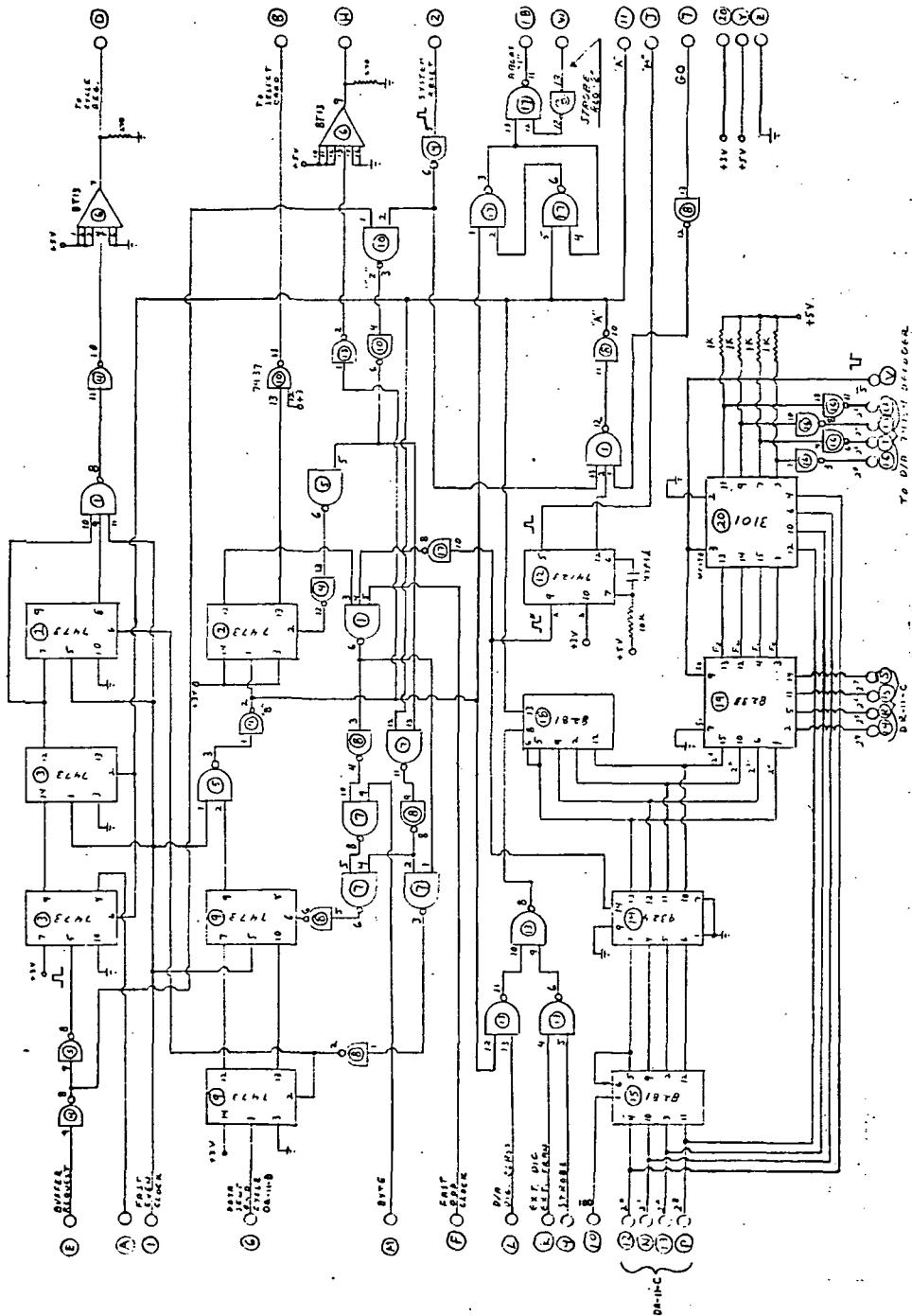


FIGURE 39. DIGITAL INPUT PROGRAMMER I (C 11)

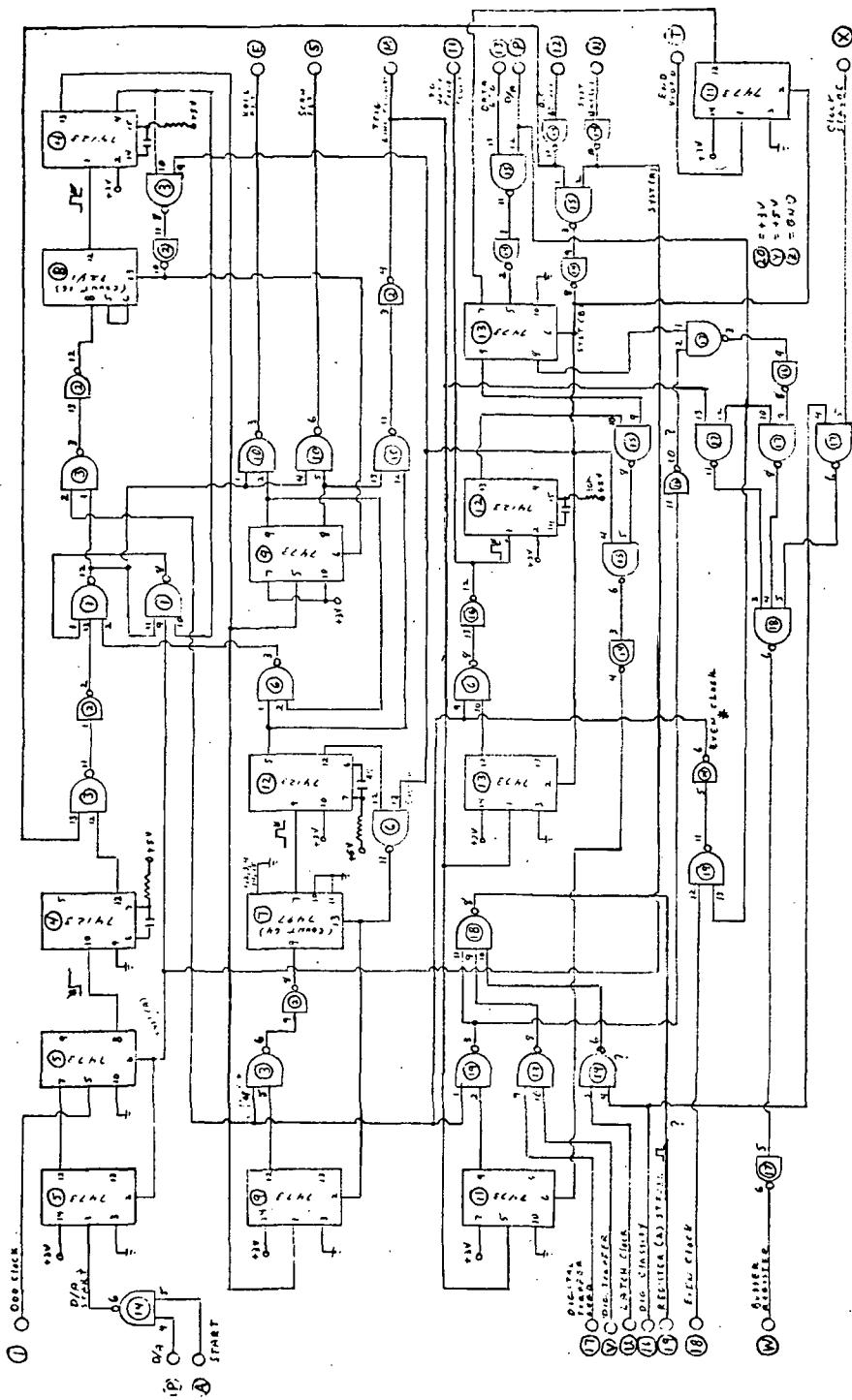


FIGURE 40. DIGITAL INPUT PROGRAMMER II (C 12)

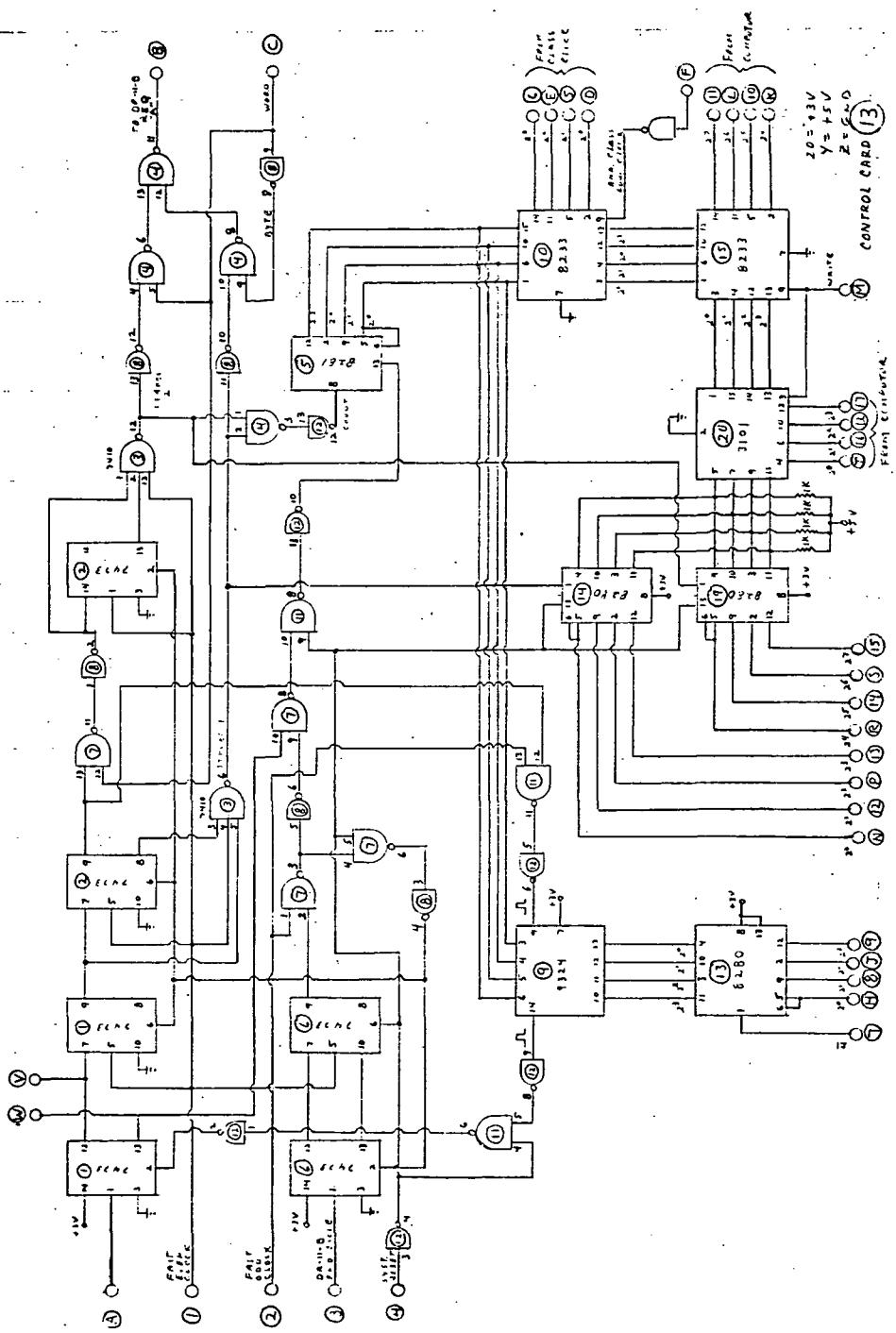


FIGURE 41. DIGITAL OUTPUT PROGRAMMER I (C 13).

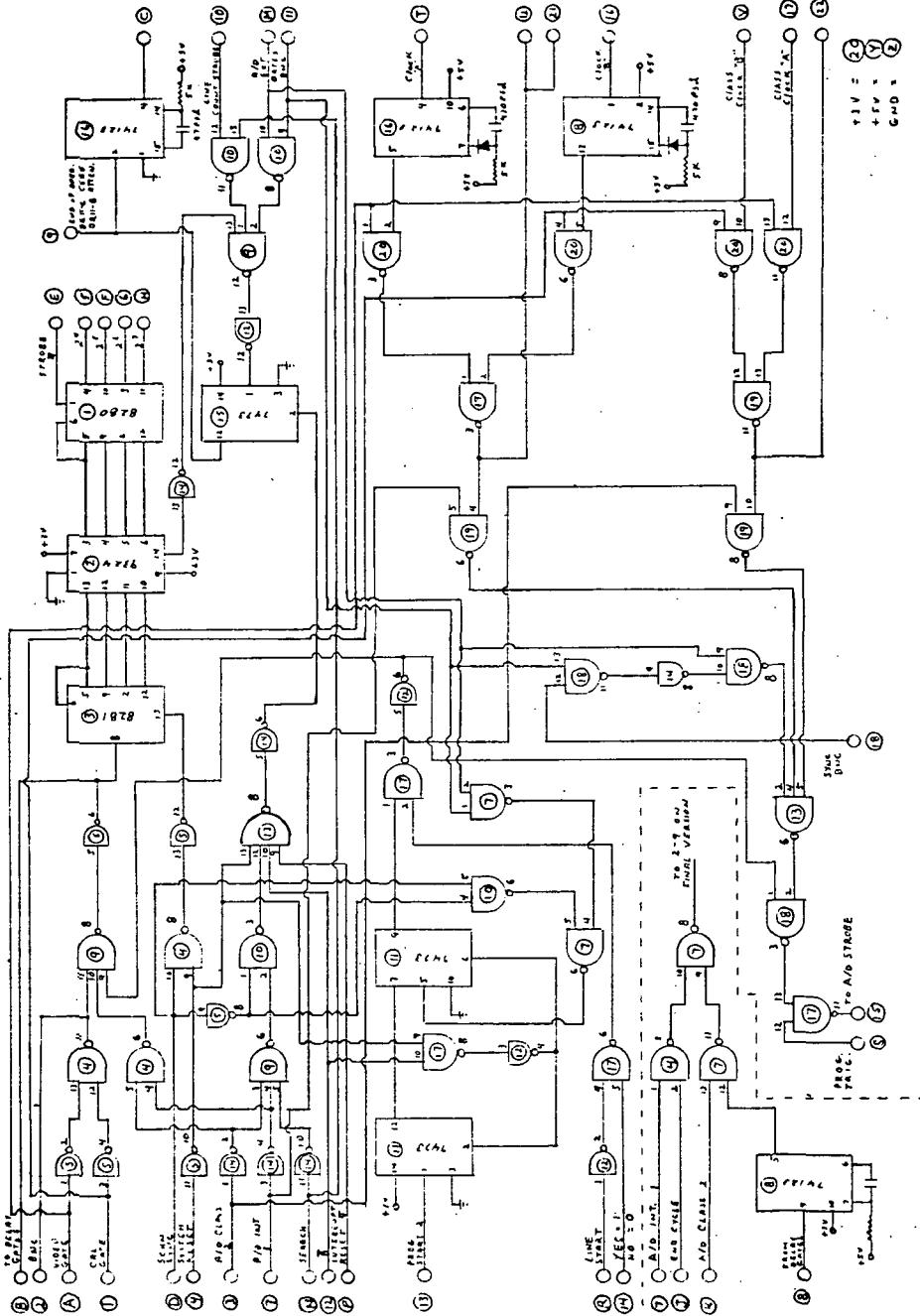


FIGURE 42. DIGITAL OUTPUT PROGRAMMER II (C 14)

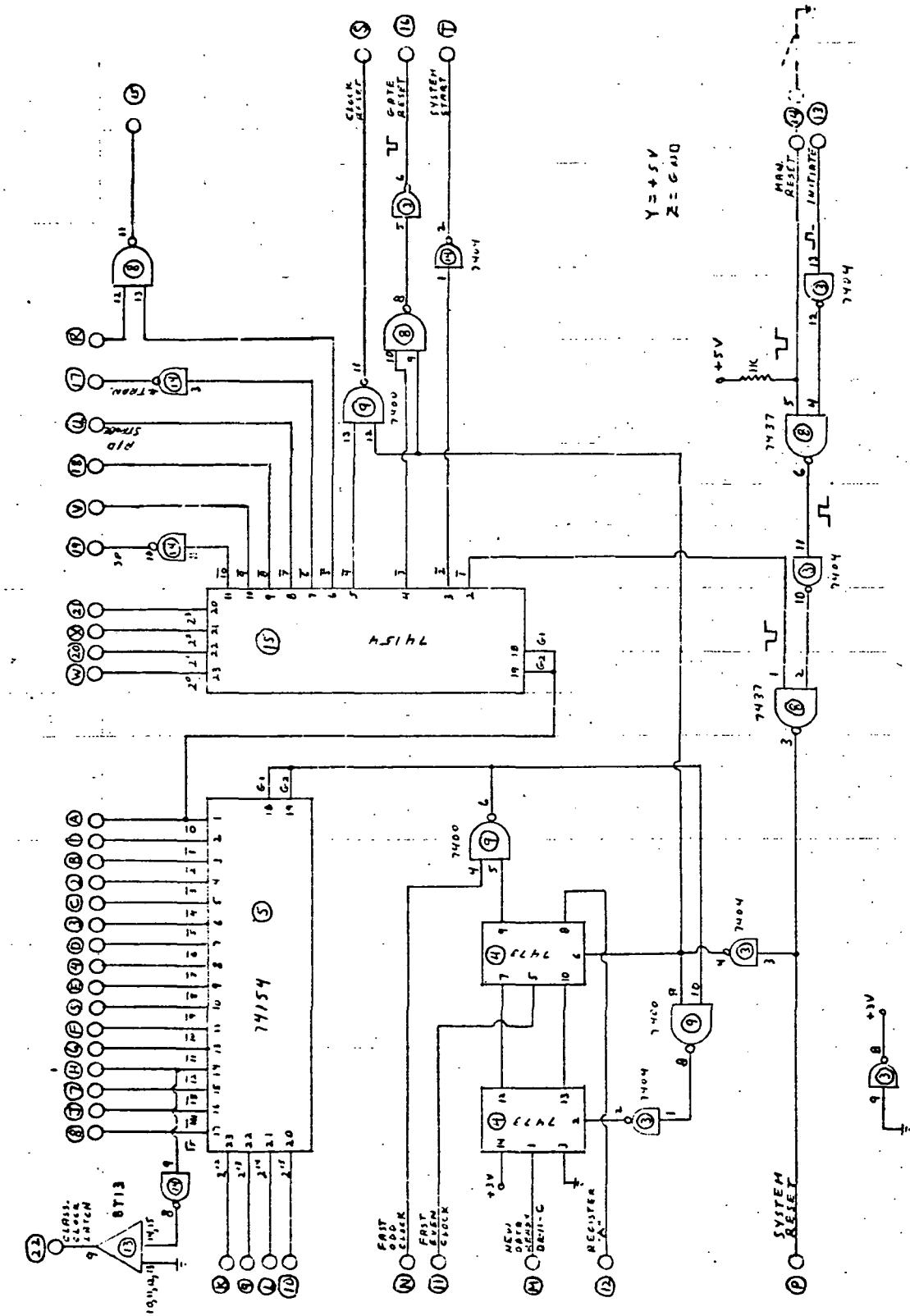


FIGURE 43. SYSTEM CONDITIONER I (C 15)

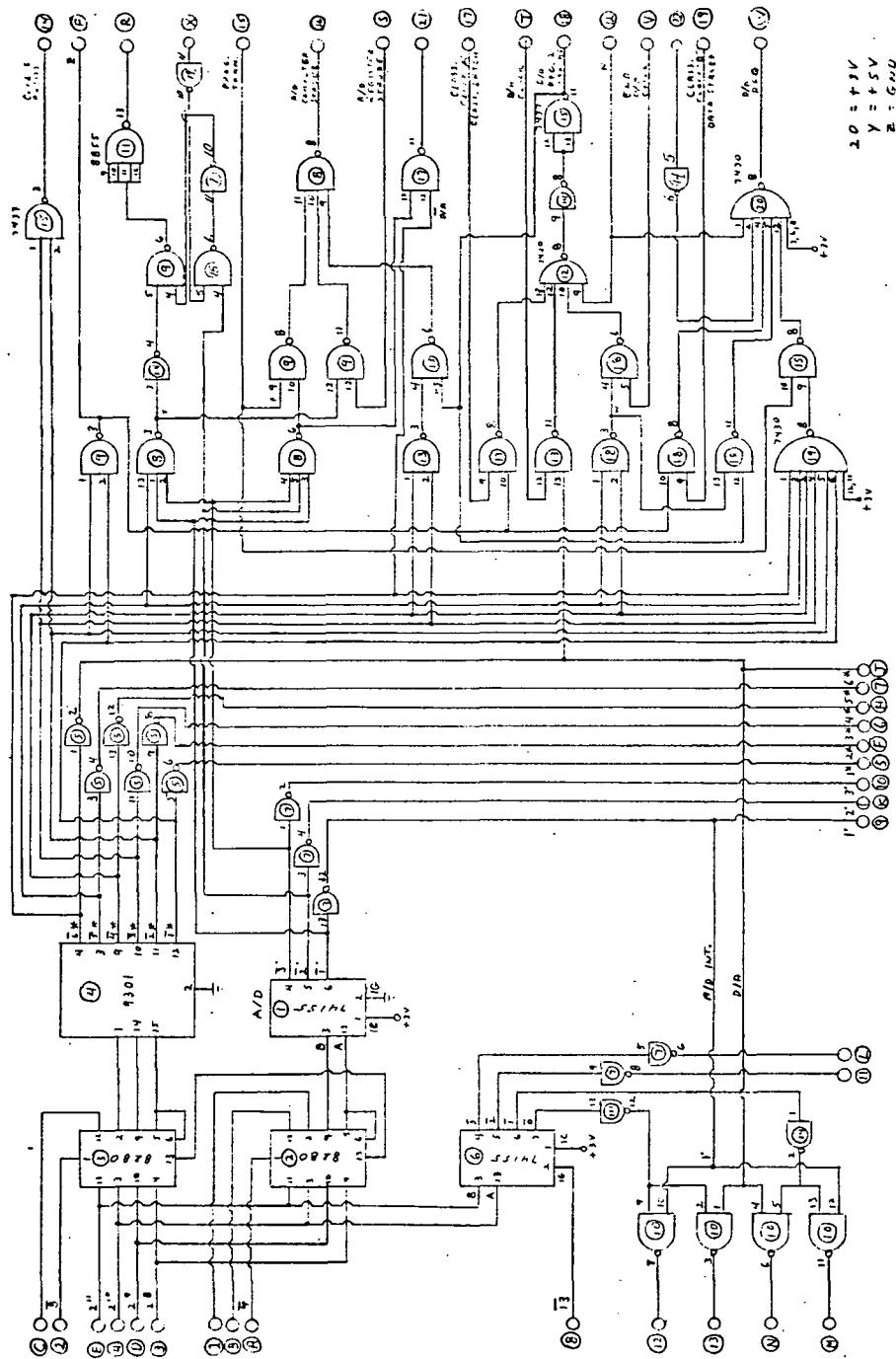


FIGURE 44. SYSTEM CONDITIONER II (C 16)



FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN

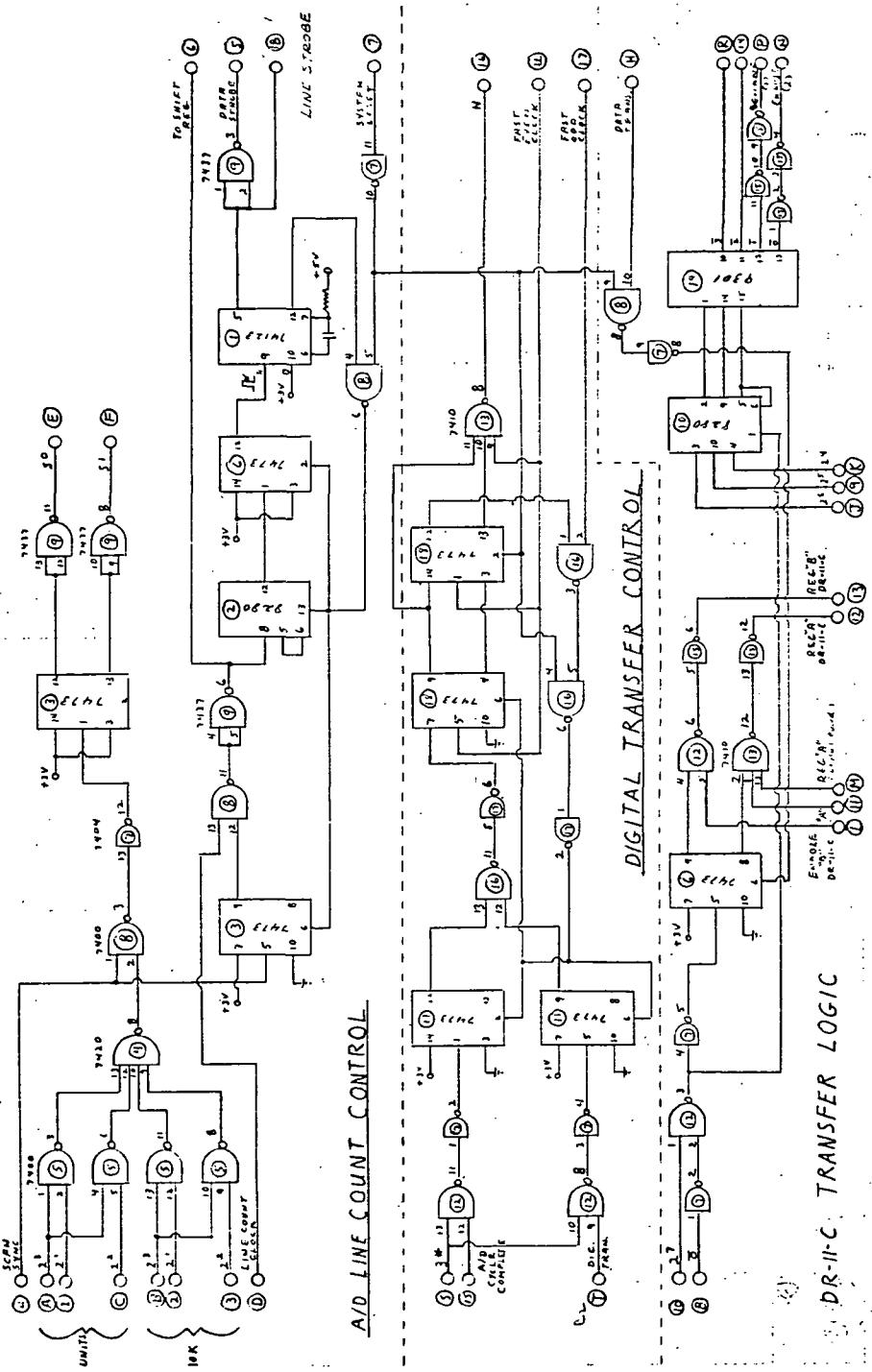


FIGURE 45. A/D LINE-COUNT CONTROL, DIGITAL TRANSFER CONTROL, AND DR-11C TRANSFER LOGIC (C 17)

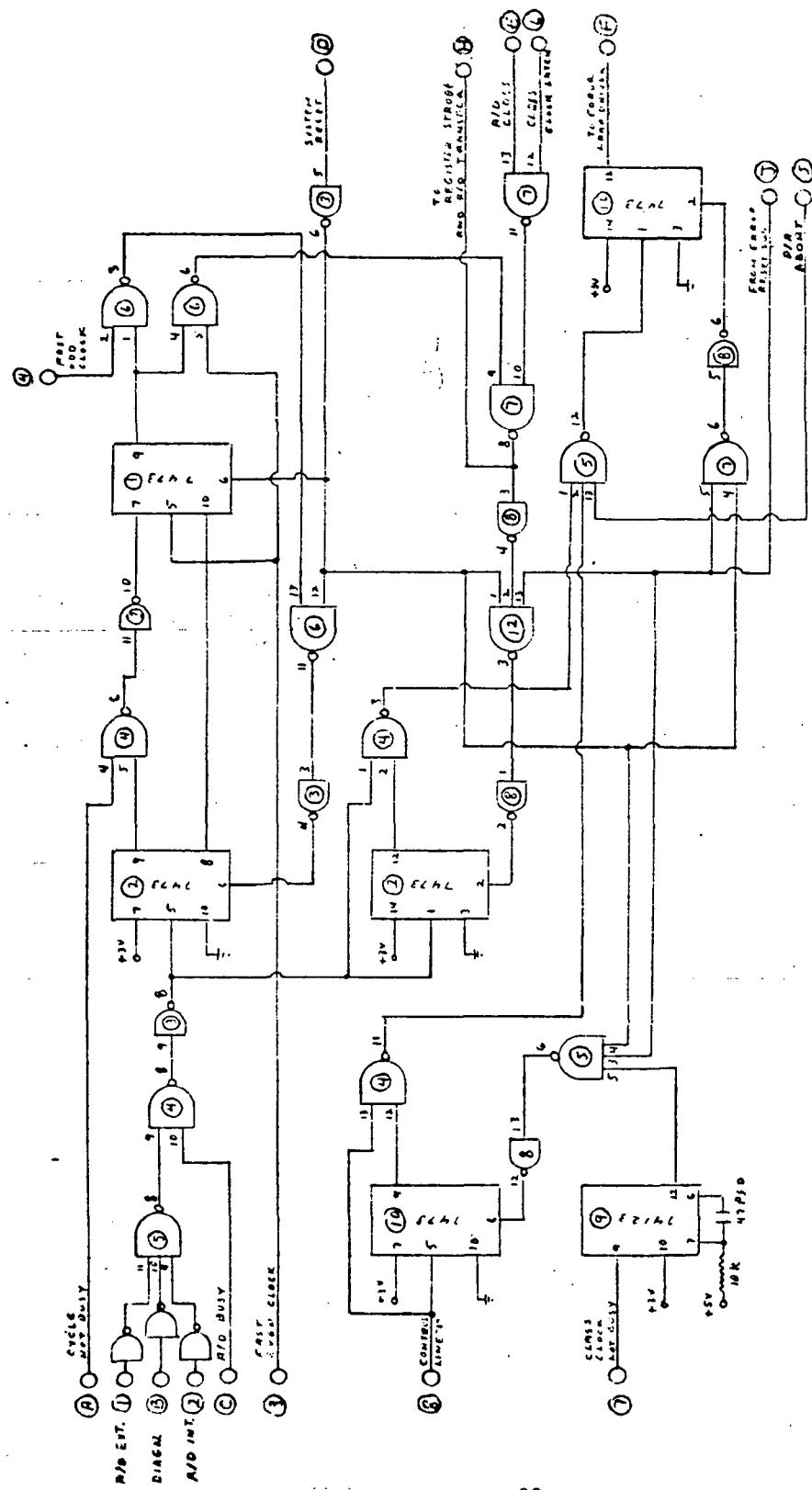


FIGURE 46. A/D WORD TRANSFER (C (18))

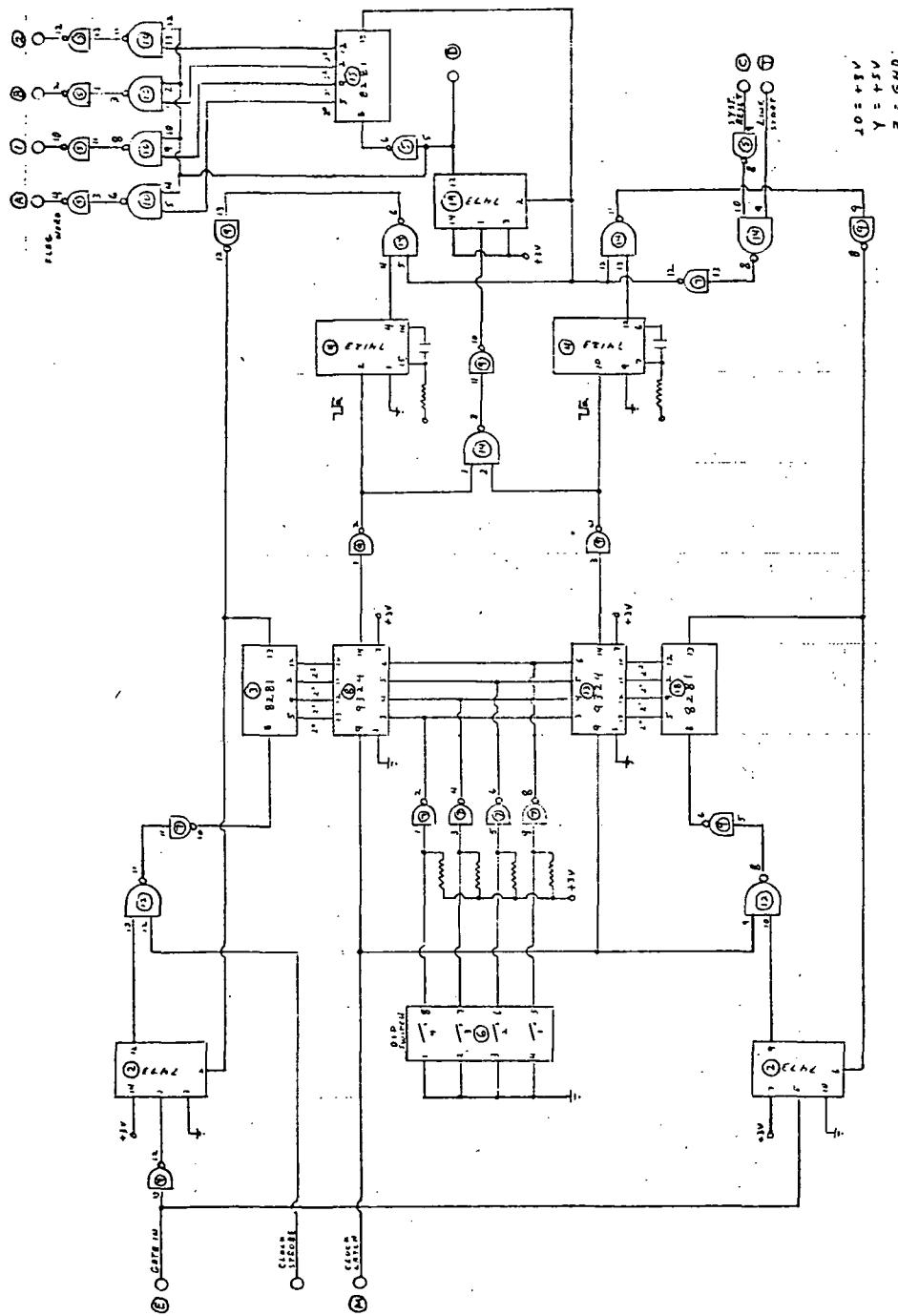


FIGURE 47. DELAY-GATE GENERATOR (C 19)

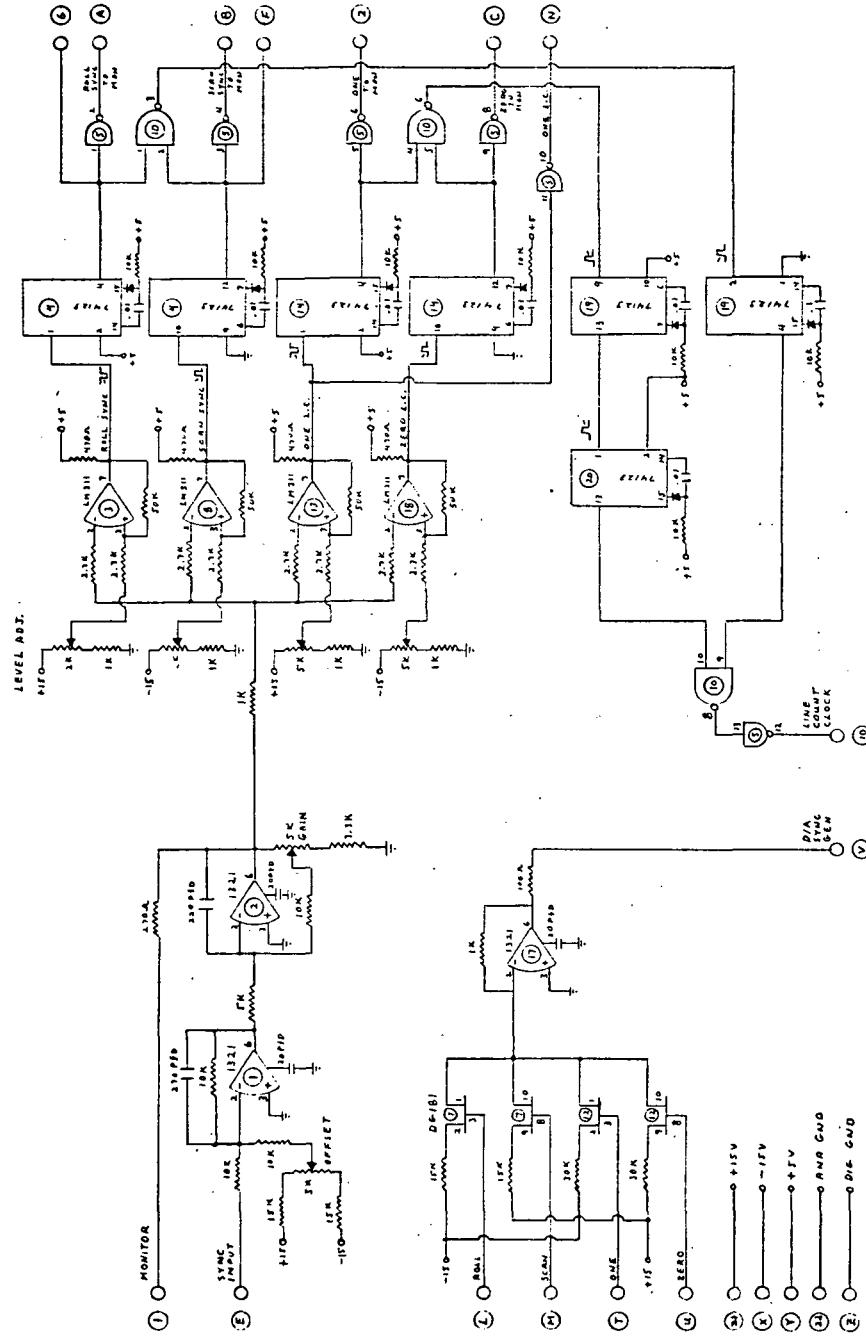


FIGURE 48. PLAYBACK SYNC AND LINE-COUNT CLOCK GENERATOR (C 20)

5

BACKPLANE INTRA-BAY WIRING

The wirewrap card files have backplanes with wirewrap connectors. These back-bay connectors have 122 pins, of which 10 are used for power and 10 for ground. Connections are shown in Fig. 49. Signal origins are shown by arrows. The various card locations are designated by odd numbers 1, 3, . . . , 25.



FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN

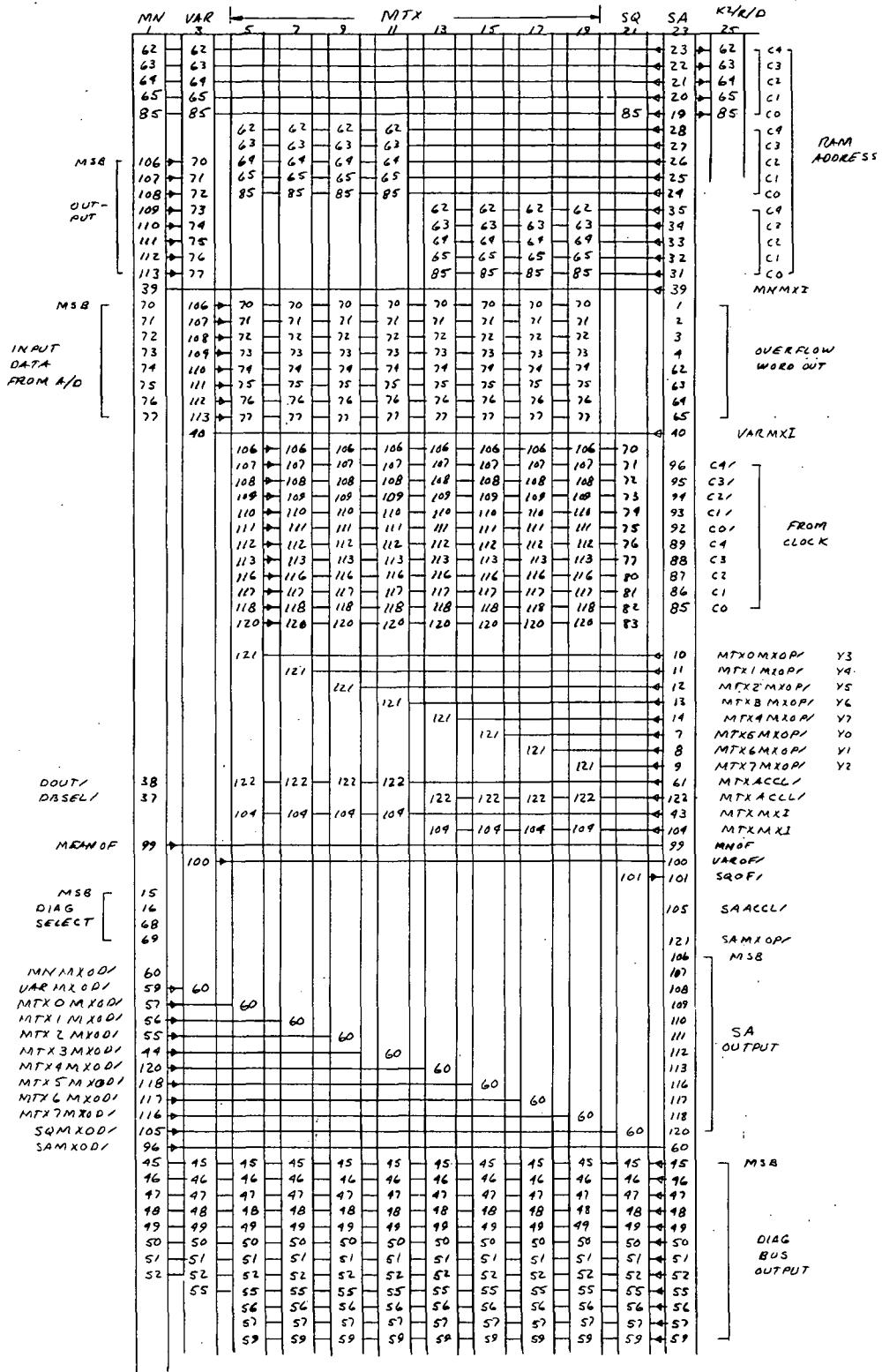
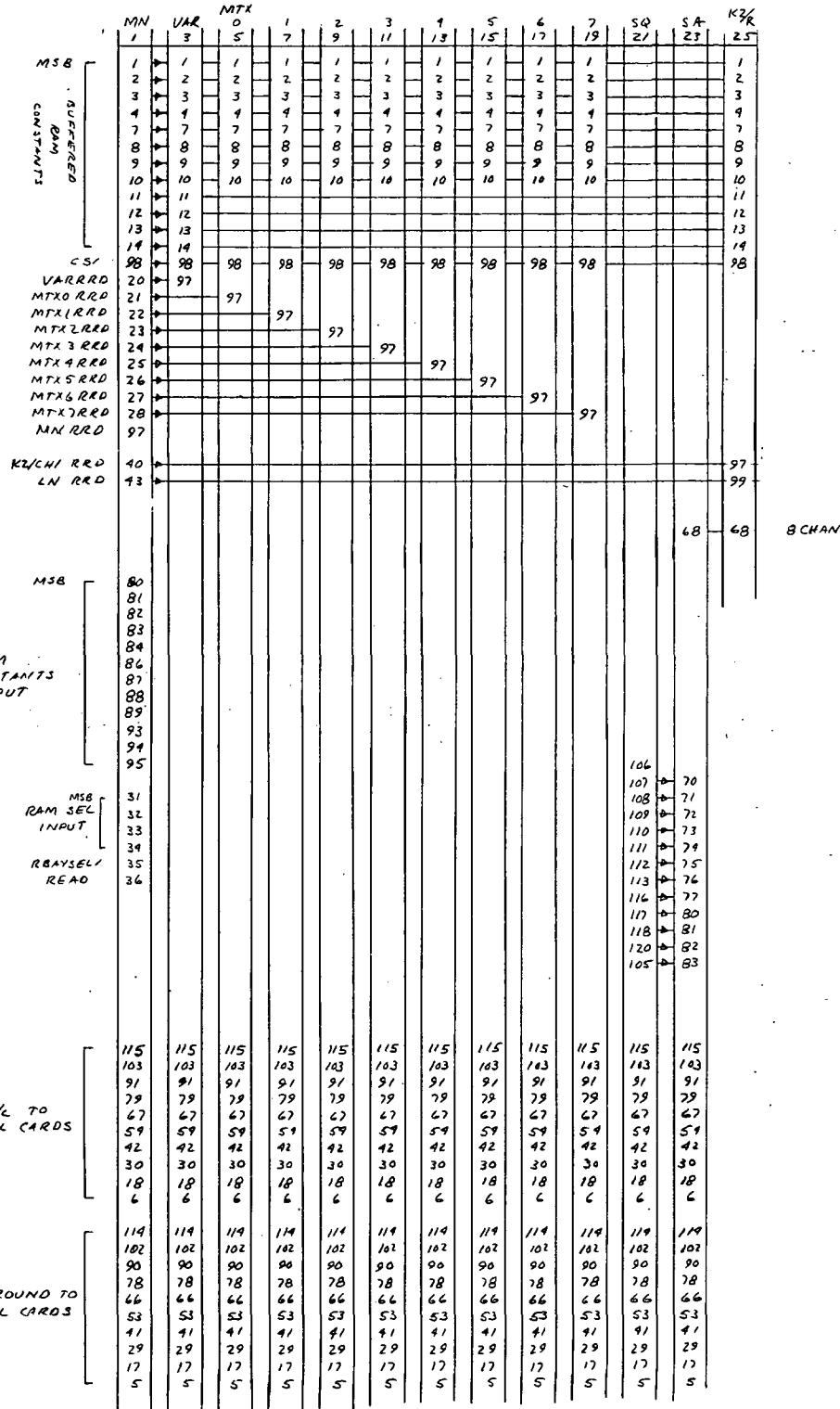


FIGURE 49. BACKPLANE INTRA-BAY WIRING (Continued)



6 SYSTEM CABLING

6.1 CABLING BETWEEN HYBRID AND CONTROL BAYS

The wiring for data and control signals flows between the hybrid and control bays including PC-board card plugs that terminate the cables interconnecting the bays. One end of each printed circuit board accommodates cable wires at tie points (T.P.) on the card; the other end of the PC board has a printed circuit connector that mates with a card slot in the connector housing associated with a particular bay.

The connector housings comprise two auxiliary files located at the rear of the control and hybrid bays, respectively. In each of these files are four card slots for the card plugs of the cables. Each slot is assigned a number (1 through 4) and a code letter (C or H) to give its position in the file and identify that file with one of the two bays (control or hybrid). Figure 50 shows overall system cabling; the table below lists the terminations of the cables that originate in the two auxiliary files.

	<u>SLOT in Aux. File</u>	<u>TERMINATION</u>
Control Bay	1-C	MIDAS CLASSIFIER
	2-C	2-H
	3-C	CONTROL PANEL
	4-C	DR-11C INTERFACE
Hybrid Bay	1-H	DR-11B INTERFACE
	2-H	2-C
	3-H	BNC CONNECTOR PANEL
	4-H	BNC CONNECTOR PANEL

The description of the interconnecting cables to and from the bays is given in Figs. 51 to 60; these figures detail the card plugs and also further describe the termination of the cables that tie into the auxiliary card files. As indicated in these diagrams, certain of the signals are buffered on the card plugs by line drivers (8T13) and line receivers (8T14). From Fig. 50 we see that cable 1C terminates eventually at the classifier. This is via a card plug that mates with a standard DEC block; then from the DEC block the signals are brought to the classifier using point-to-point wirewrap. Figure 55 shows the layout of the card plugs associated with the DEC block while Fig. 56 gives the block configuration. It may be noted that the cables originating from slots 3-H and 4-H are not detailed in this section.

6.2 CABLING BETWEEN CLASSIFIER AND COMPUTER

As indicated in the system cabling diagram (Fig. 50), a cable runs from the classifier to a DR-11B interface; it is used to carry information (e.g., RAM load, classifier output, diagnostic info) to and from the classifier through the DEC block. At the classifier end, this cable terminates in a card plug which connects to a DEC block (for block layout, see Fig. 56). The classifier

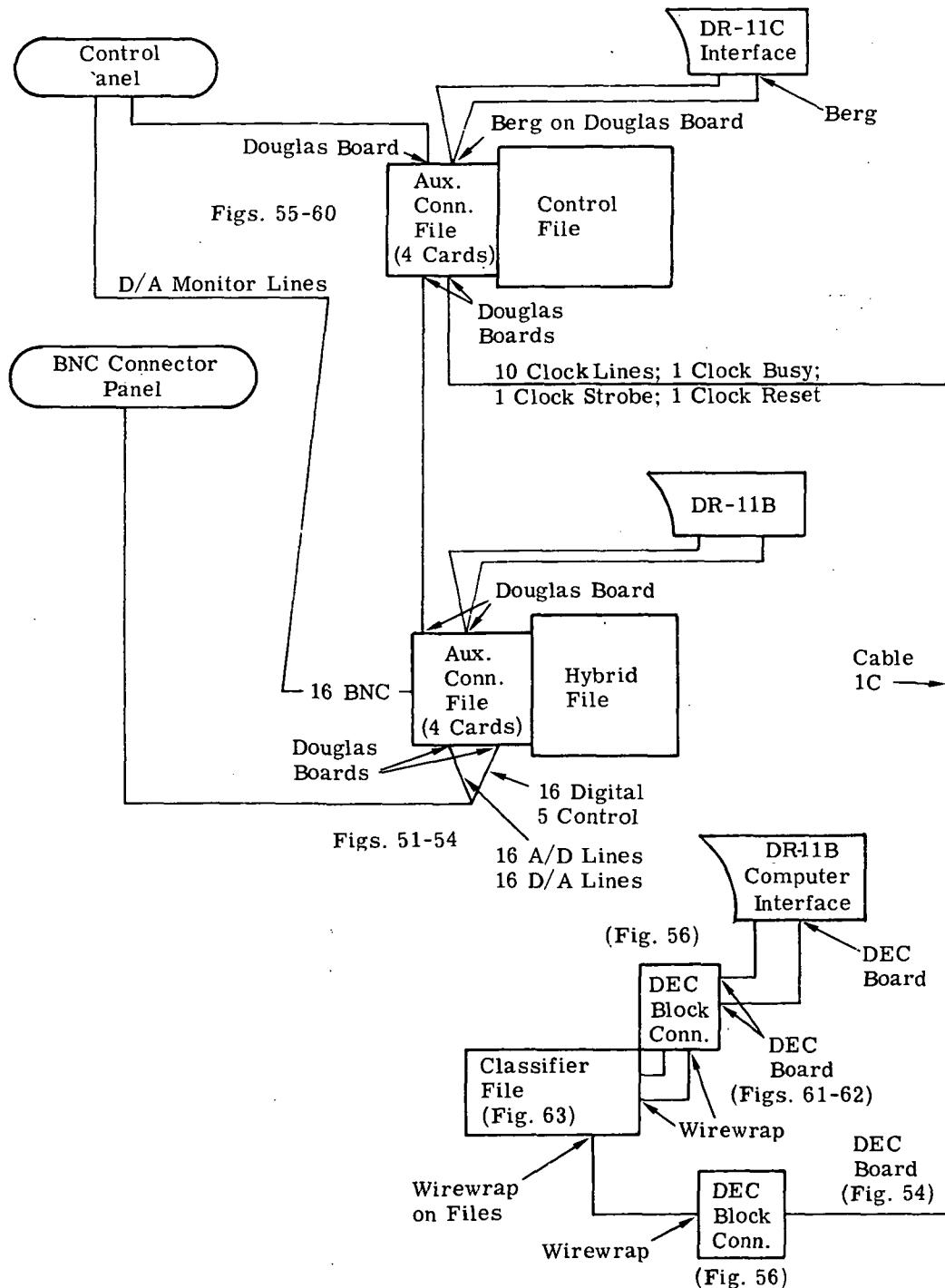


FIGURE 50. SYSTEM-CABLING DIAGRAM

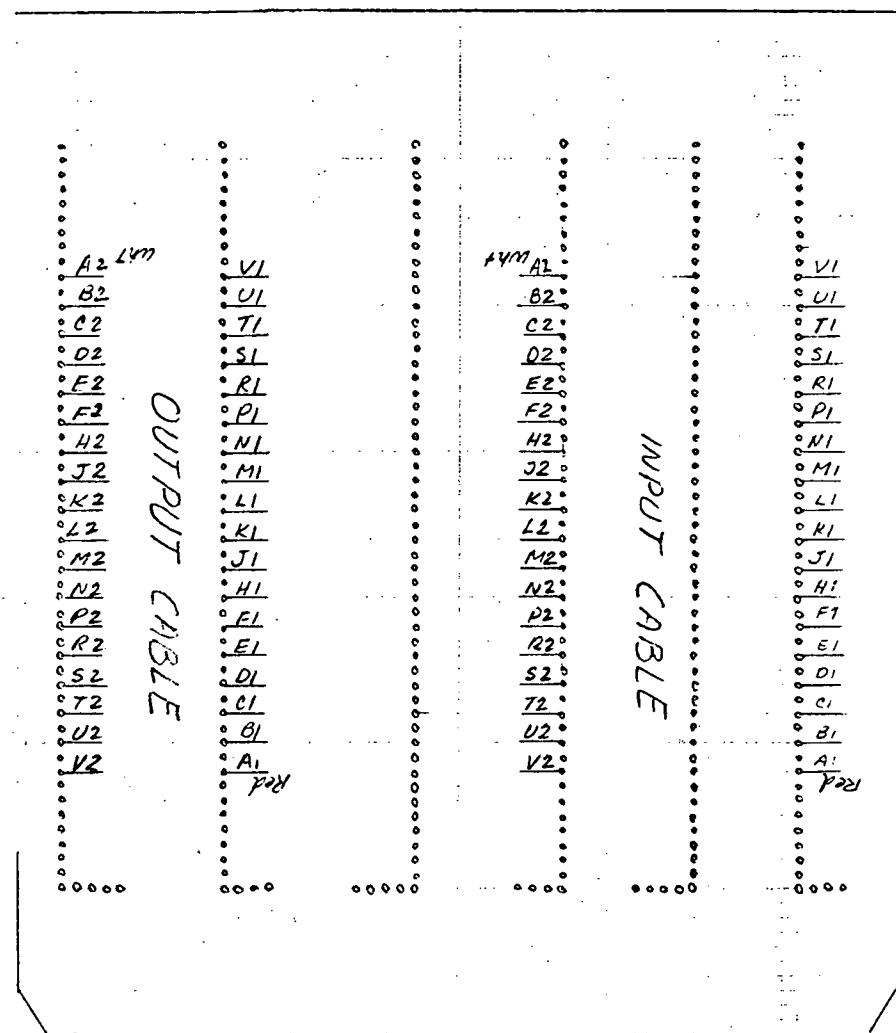


FIGURE 51. PHYSICAL LAYOUT OF PLUG CARD 1-H



FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN

No.	DR-11B Pin	Input Cable Connector	Function	No.	DR-11B Pin	Output Cable Connection	Function
1.	A1	A	Cycle Request A	1.	V1	N	(GO)
2.	B1	1	End Cycle Out	2.	F2	12	C1 Control
3.	C1	B	Data 00	3.	H1	P	Function 2
4.	D1	2	Data 01	4.	H2	13	Single Cycle
5.	D2	C	Data 02	5.	J2	R	Function 3
6.	E1	3	Data 03	6.	K1	14	Data 11
7.	E2	D	Data 04	7.	K2	S	Data 15
8.	F1	4	Data 05	8.	L1	15	Data 09
9.	F2	E	Data 06	9.	L2	T	Data 14
10.	H1	5	Data 07	10.	M1	16	Data 07
11.	H2	F	Data 08	11.	M2	U	Data 13
12.	J1	6	Data 09	12.	N1	17	Data 05
13.	J2	H	Data 10	13.	N2	V	Data 12
14.	K1	7	Data 11	14.	P1	18	Data 03
15.	K2	J	Data 12	15.	P2	W	Data 10
16.	L2	8	Data 13	16.	R1	19	Data 01
17.	M1	K	ATTEN.	17.	R2	X	Data 08
18.	M2	9	Data 14	18.	S1	20	Data 00
19.	N2	L	Data 15	19.	S2	Y	Data 06
20.	S2	10	Busy	20.	T2	21	Data 04
21.	T1	M	GND	21.	U1	Z	Cycle Request B
22.	U2	11	INIT.	22.	U2	22	Data 02

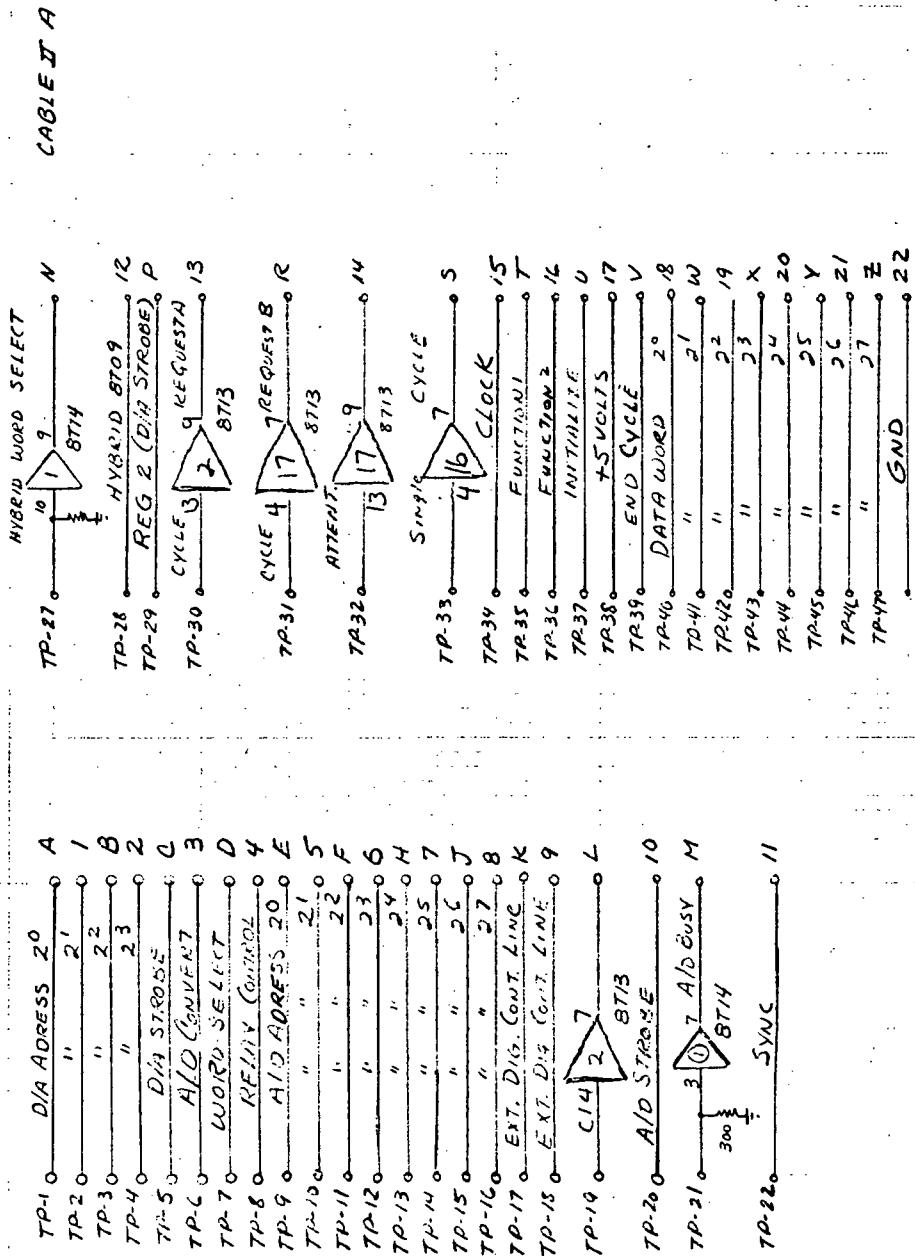
Note: Gnd. (T1) on both input and output cable to card.

Note: Gnd (F1) and output cable to gnd on card.

Figure (a)

Figure (b)

FIGURE 52. OUTPUT CONNECTOR WIRING OF PLUG CARD (1-H)



Note: GND CARRIED SEPARATELY FROM
 FLAT CABLE
 P/N 22.70 GND bus on card

FIGURE 53. WIRING OF PLUG CARD 2-H

NOTE: ON PLATE CHART, RED IS NUMBER #1

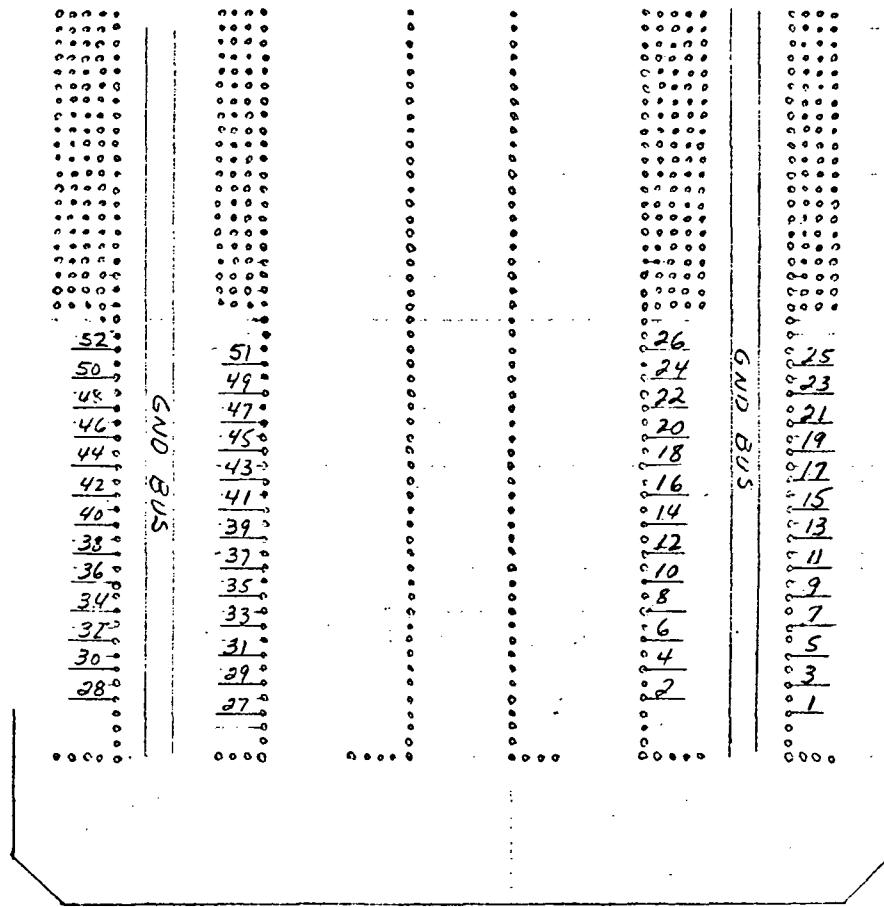
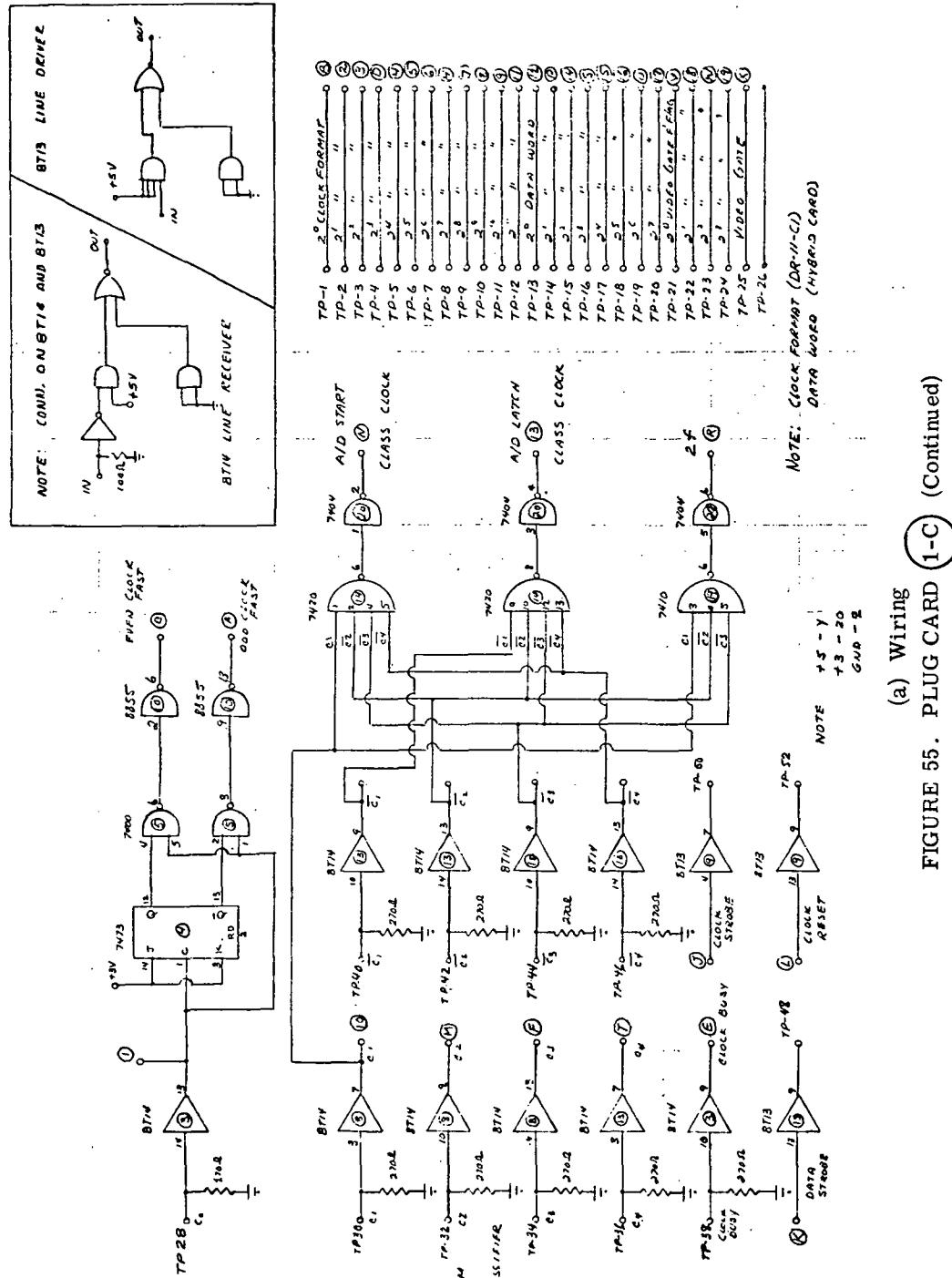
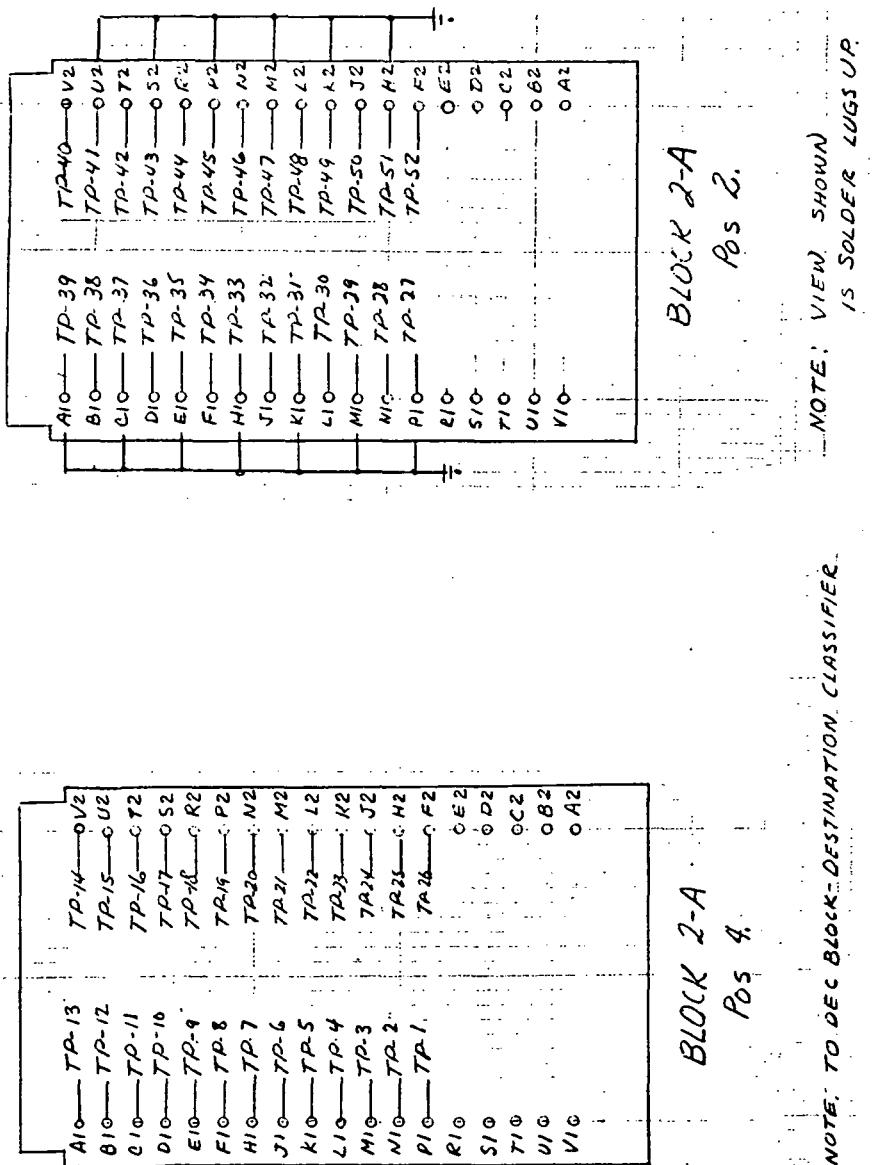


FIGURE 54. PHYSICAL LAYOUT OF PLUG CARDS 2-H AND 2-C





(b) DEC Block Termination of Plug Card 1-C

FIGURE 55. PLUG CARD 1-C (Continued)

BLOCK CONNECTOR
 2-A Position 2

		A1	Gnd.	A2		A1	2^0	Data Word	A2
B1	Clock Busy	B1		B2		B1	2^{11}	Data Format	B2
C1	Gnd.	C1		C2		C1	2^{10}	Data Format	C2
D1	C4	D1		D2		D1	2^9	Data Format	D2
E1	Gnd.	E1		E2		E1	2^8	Data Format	E2
F1	C3	F1		F2	Clock Reset	F1	2^7	Data Format	F2
H1	Gnd.	H1		H2	Gnd.	H1	2^6	Data Format	H2
J1	C2	J1		J2	Clock Strobe	J1	2^5	Data Format	J2
K1	Gnd.	K1		K2	Gnd.	K1	2^4	Data Format	K2
L1	C1	L1		L2	Data Strobe	L1	2^3	Data Format	L2
M1	Gnd.	M1		M2	Gnd.	M1	2^2	Data Format	M2
N1	C \emptyset	N1		N2	$\overline{C_4}$	N1	2^1	Data Format	N2
P1	Gnd.	P1		R1	$\overline{C_3}$	P1	2^0	Data Format	P2
S1		S1		T1		R1		Data Word	S2
T1		T2	$\overline{C_2}$	U1				Data Word	T2
U1		U2	Gnd.	V1	$\overline{C_1}$	U1		Data Word	U2
V1		V2		V1		V1		Data Word	V2

(c) Connector Wiring of DEC Block Termination

FIGURE 55. PLUG CARD (1-C) (Concluded)

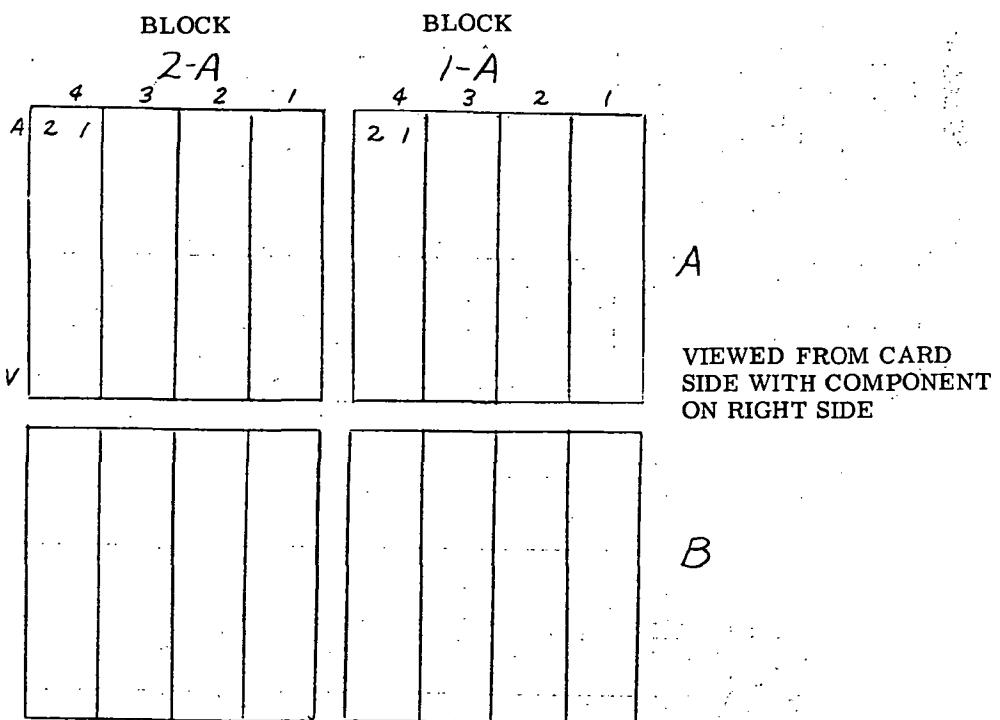


FIGURE 56. DEC BLOCK LAYOUT

TABLE II B

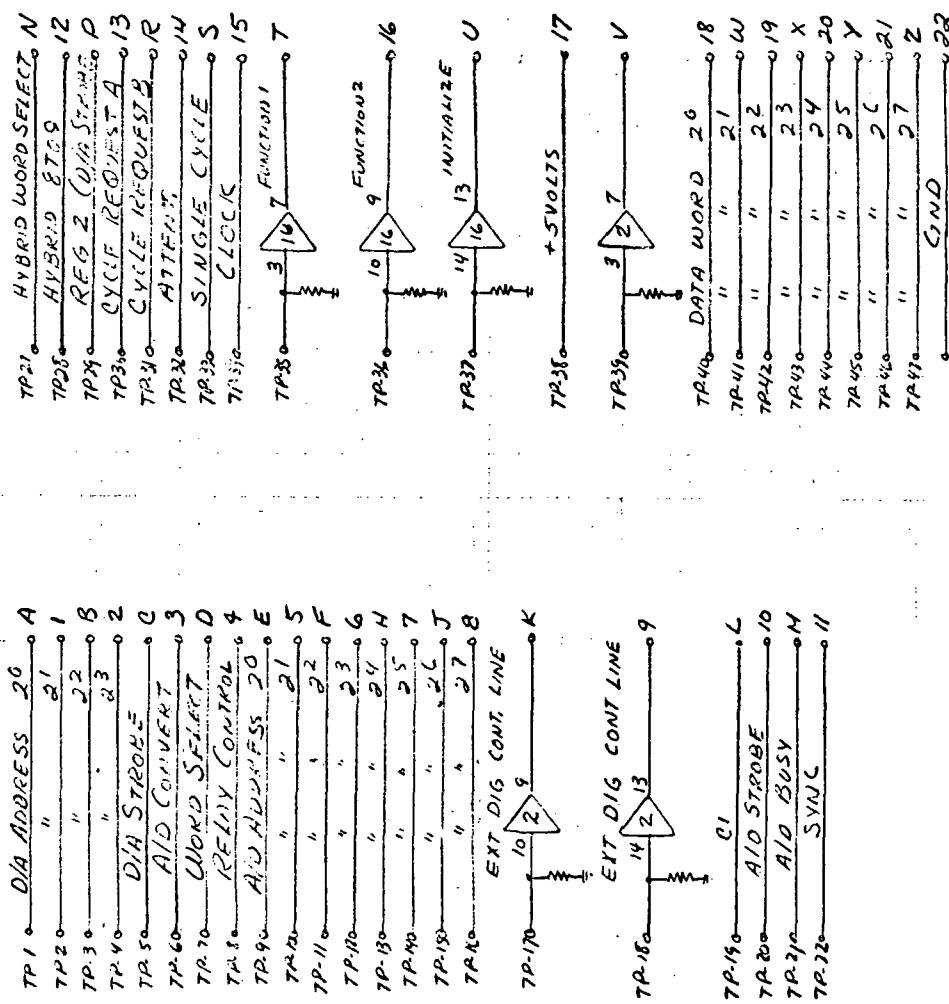


FIGURE 57. WIRING OF CARD 2-C

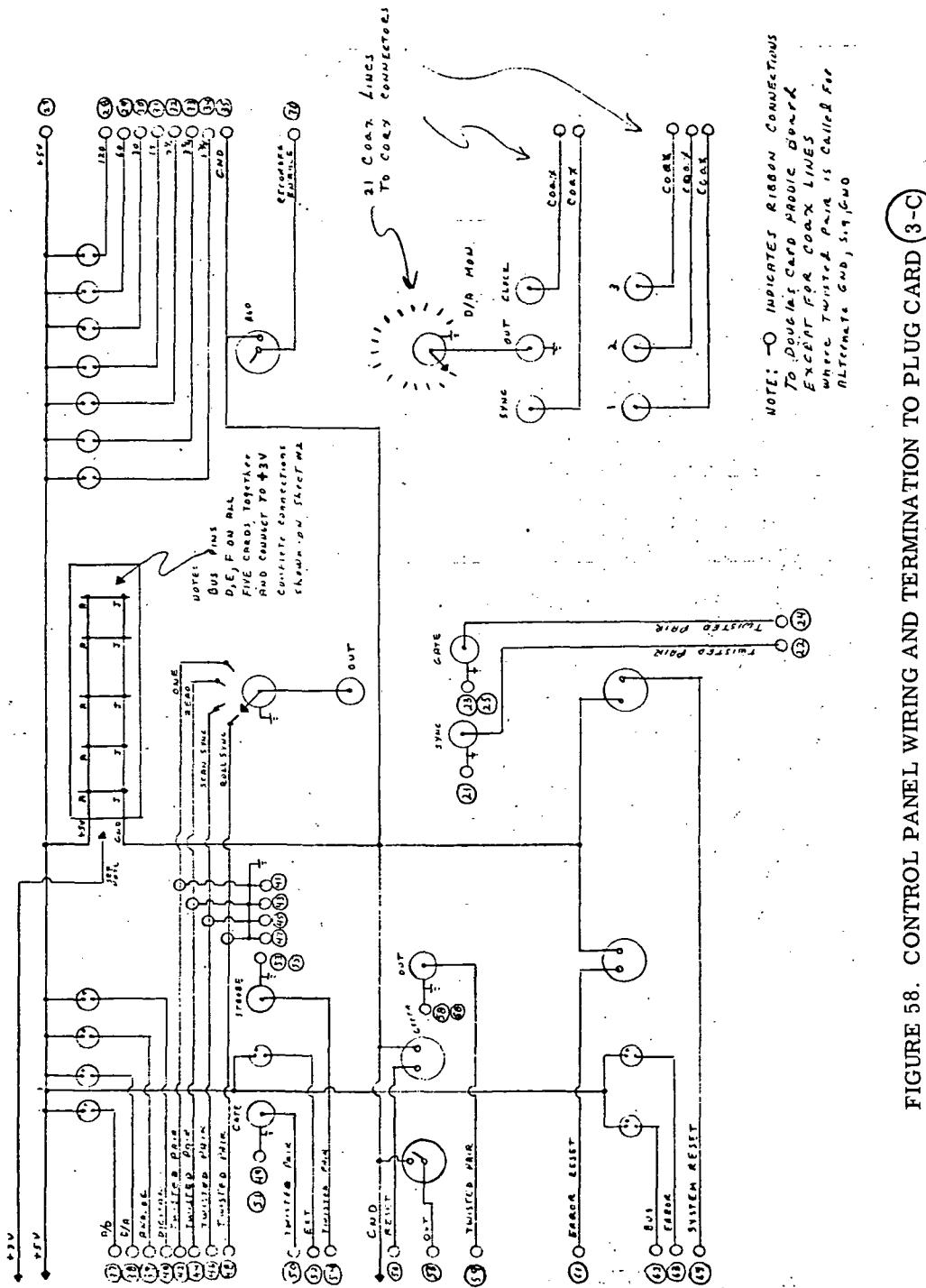


FIGURE 58. CONTROL PANEL WIRING AND TERMINATION TO PLUG CARD (3-C)

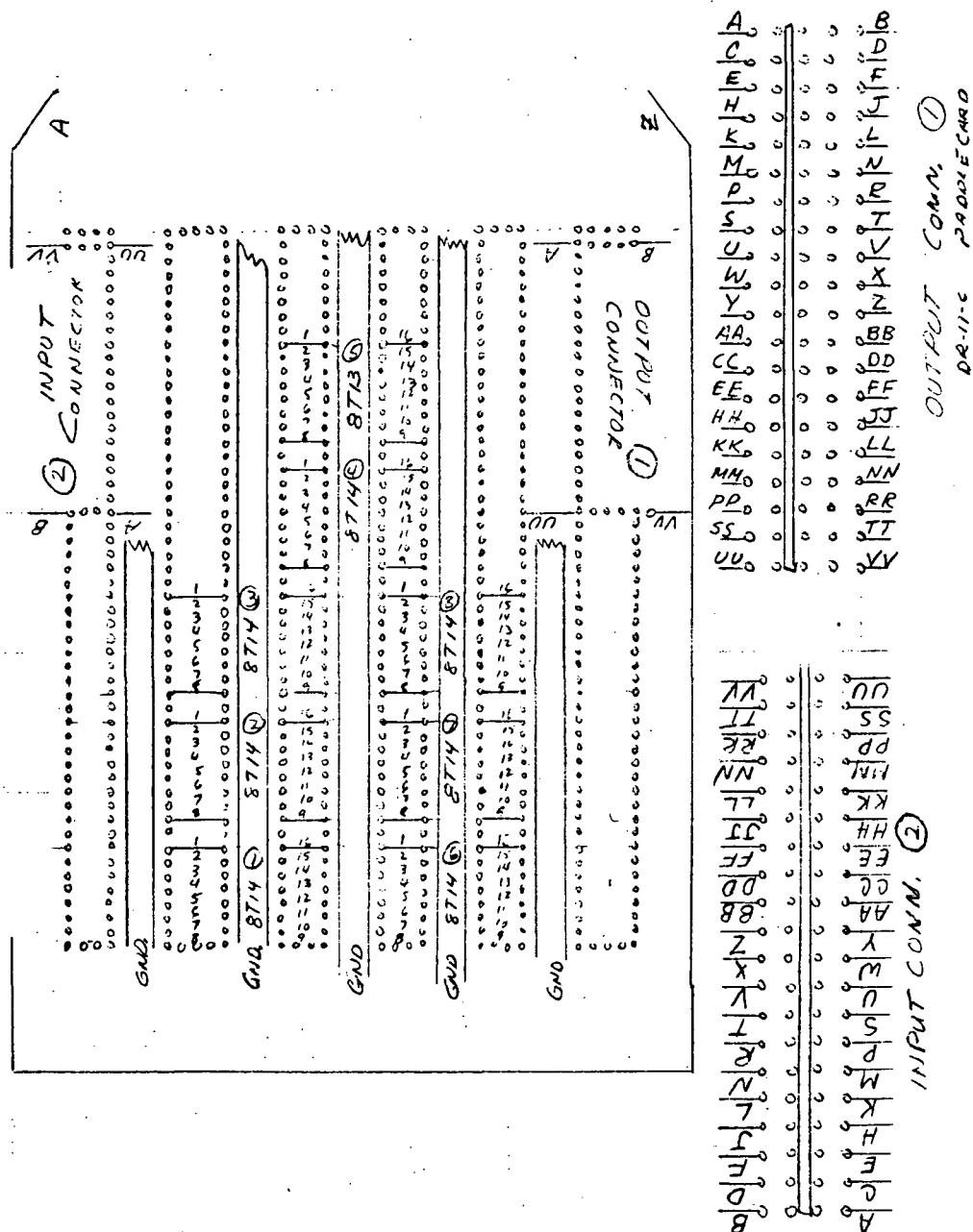


FIGURE 59. PHYSICAL LAYOUT OF PLUG CARD (4-C)



FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN

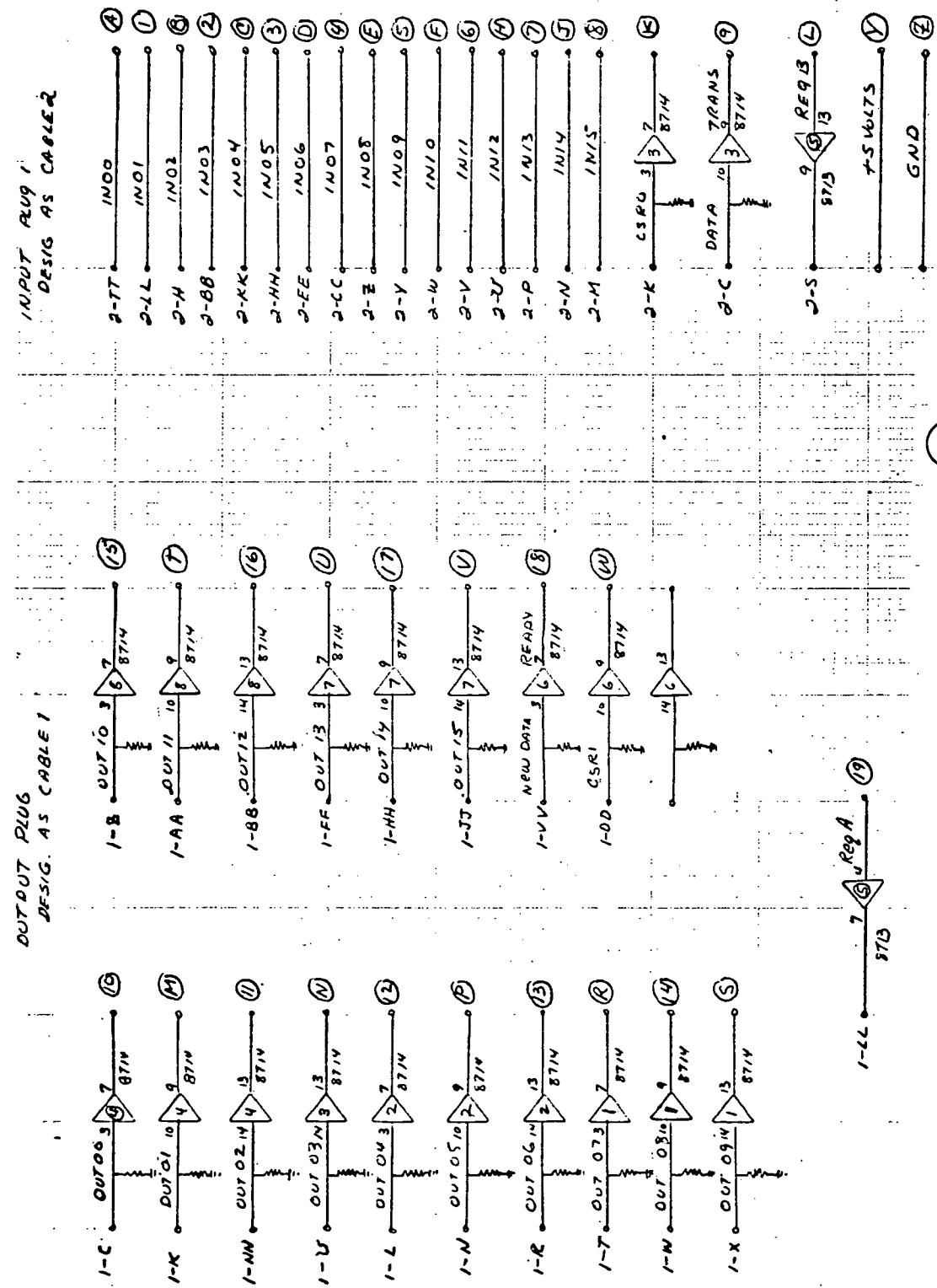


FIGURE 60. WIRING OF CARD (4-C)



FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN

connection to the computer via the DR-11B is through line drivers and receivers located on the card plugs; these cards are detailed in Figs. 61 and 62. The classifier inter-bay wiring and cabling to the DEC block are shown in Fig. 63.



FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN

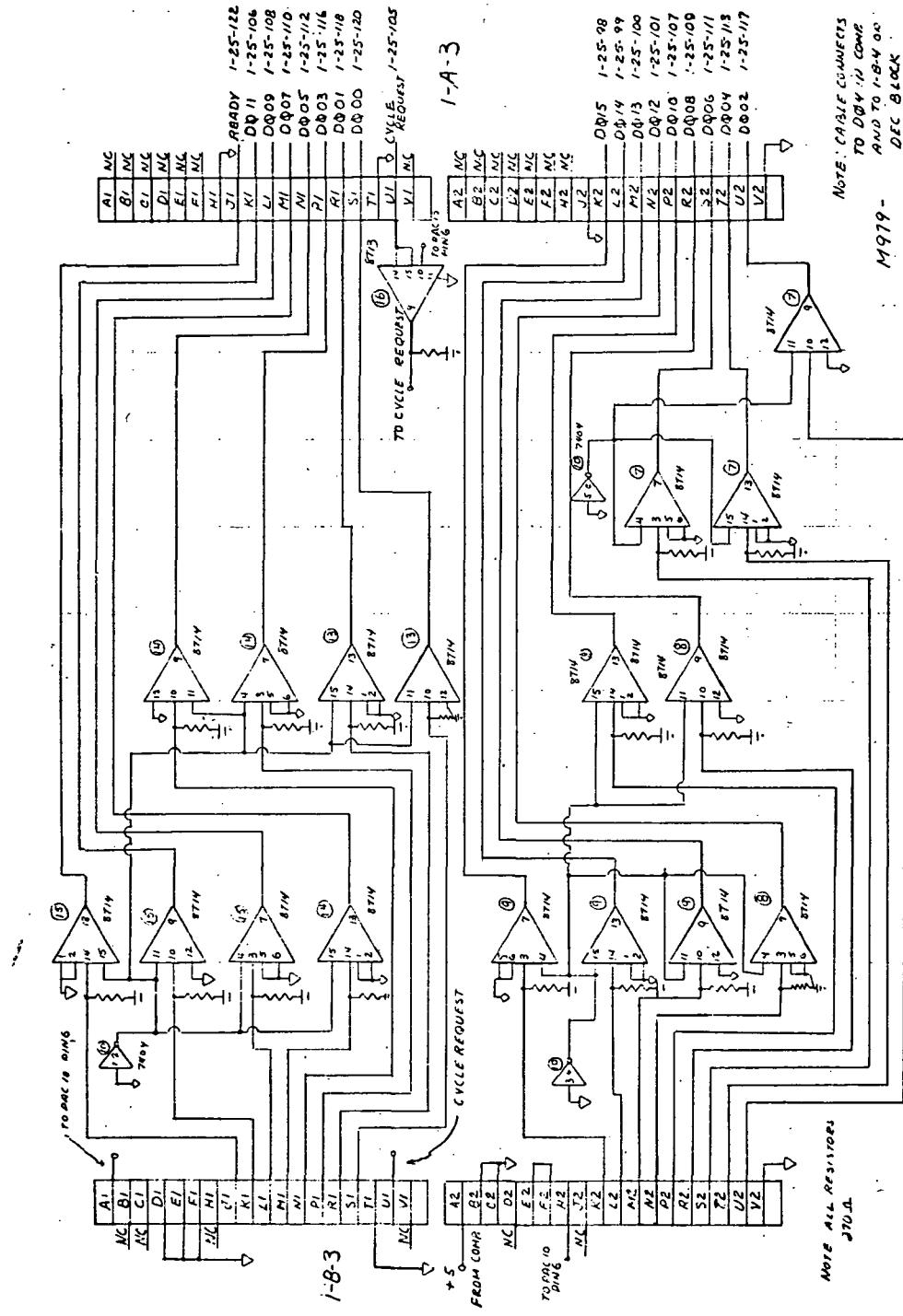


FIGURE 61. CABLE TERMINATIONS FOR DATA TRANSFER FROM COMPUTER TO CLASSIFIER



FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN

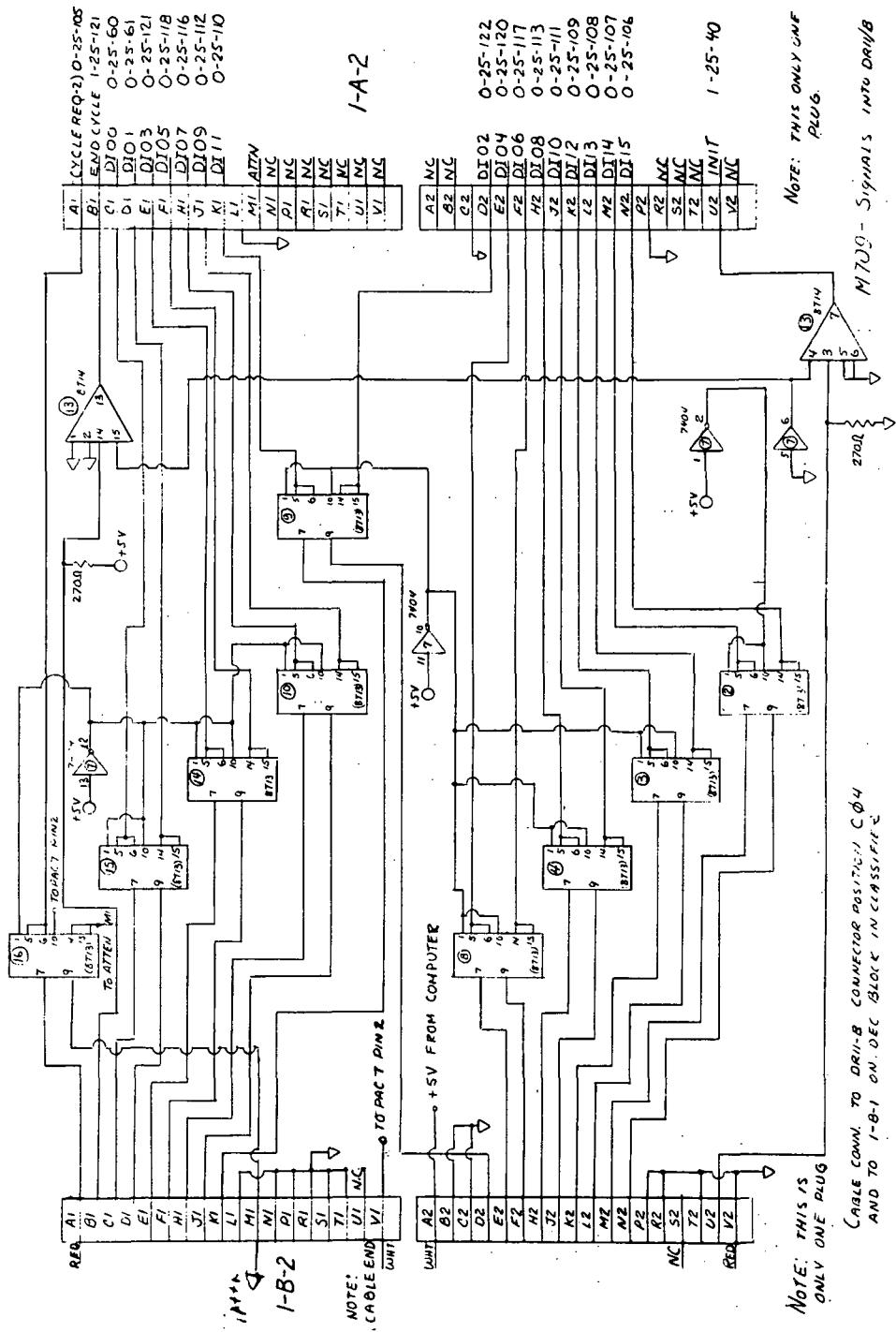
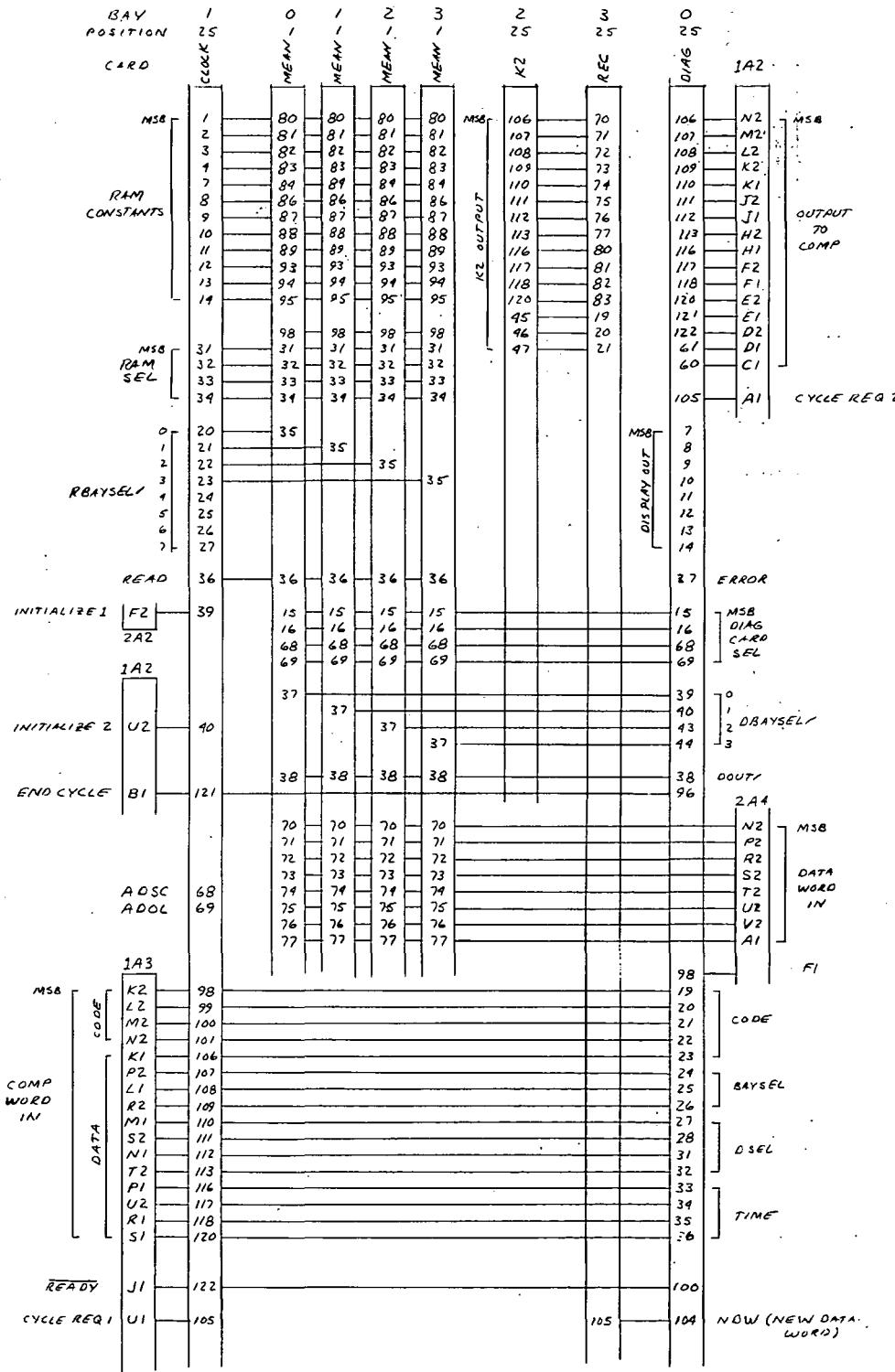


FIGURE 62. CABLE TERMINATIONS FOR DATA TRANSFER TO COMPUTER FROM CLASSIFIER



(a) Sheet 1
FIGURE 63. INTER-BAY WIRING (Continued)



FORMERLY WILLOW RUN LABORATORIES, THE UNIVERSITY OF MICHIGAN

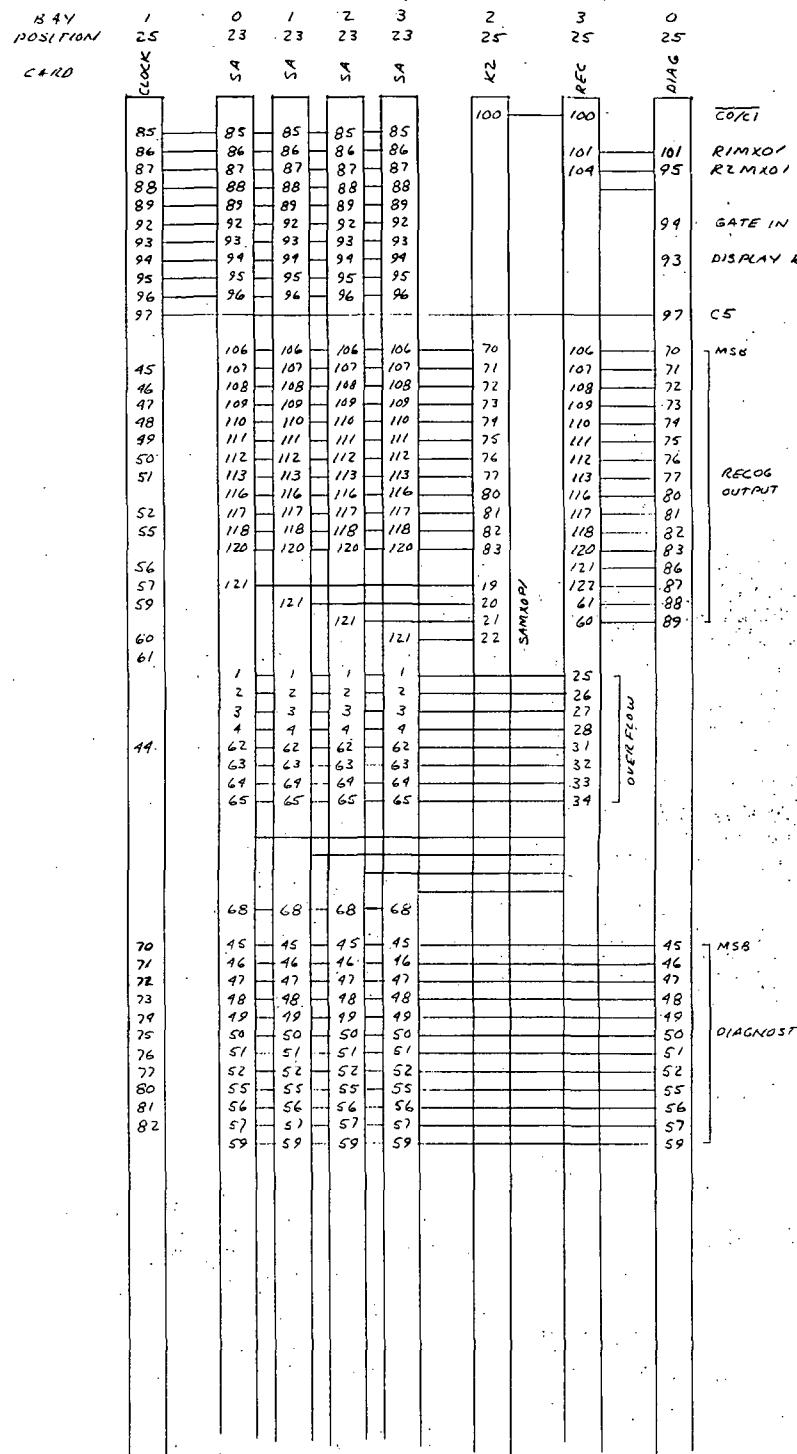


FIGURE 63. INTER-BAY WIRING (Concluded)

DISTRIBUTION LIST

NASA Langley Research Center
Hampton, VA 23665

ATTN: Report & Manuscript Control Office, Mail Stop 180A (1)
ATTN: Raymond L. Zavasky, Mail Stop 115 (1)
ATTN: Technology Utilization Office, Mail Stop 193A (1)
ATTN: William M. Howle, Jr., Mail Stop 470 (10)

NASA Ames Research Center
Moffett Field, CA 94035

ATTN: Library, Mail Stop 202-3 (1)

NASA Flight Research Center
P.O. Box 273
Edwards, CA 93523

ATTN: Library (1)

NASA Goddard Space Flight Center
Greenbelt, MD 20771

ATTN: Library (1)

NASA Lyndon B. Johnson Space Center
2101 Webster Seabrook Road
Houston, TX 77058

ATTN: Library, Code JM6 (1)

Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, CA 91103

ATTN: Library, Mail 111-113 (1)

NASA Lewis Research Center
21000 Brookpark Road
Cleveland, OH 44135

ATTN: Library, Mail Stop 60-3 (1)

NASA John F. Kennedy Space Center
Kennedy Space Center, FL 32899

ATTN: Library, IS-DOC-1L (1)

NASA Marshall Space Flight Center
Huntsville, AL 35812

ATTN: Library (1)

National Aeronautics & Space Administration
Washington, D.C. 20546

ATTN: Kss-10/Library (1)
ER/NASA Headquarters (1)

NASA Scientific & Technical Information Facility
P.O. Box 33
College Park, MD 20740 (plus 1 reproducible) (27)